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TIMING MARGIN MEASUREMENT USING A LASER TECHNIQUE

University of Central Florida

Harold K. Brown, Glenn C. Fuller, Shane S. Clammae

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13. ABSTRACT (Maximum 200 words) This report describes a non-contact technique for obtaining information about the timing margins of internal signal paths in CMOS circuits. A controlled photocurrent is injected by spot illumination of an OFF transistor drain loading a node. The collected photocurrent aids or opposes transistors driving the node. This increases (or decreases) node switching times, and may manifest as a change in the maximum operating frequency of the overall circuit. An approach for extracting timing margin values from plots of maximum operating frequency vs illumination intensity has been developed, which does not require estimation of the drive strength or capacitive load of the node tested. Theory, implementation details, difficulties, and test results on a CMOS microprocessor are discussed.				
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FINAL REPORT

TIMING MARGIN MEASUREMENT USING A LASER TECHNIQUE

Product specifications relating to timing, such as the access time of a memory or the maximum clock frequency of a microprocessor are important in the marketplace. These parameters are carefully defined and specified on data sheets, and can be verified by electrical test. It follows that internal timing specifications and testing methods are equally important, at least to the device designer, but they are not generally specified on data sheets, and are not easily measured.

This information would be useful in assessing the "quality of design" according to criteria involving internal timing robustness. Easy access to this information using improved device test methods would enable interesting experimental study of the relationships between overall timing robustness and several factors, including starting materials, processing, device electrical design, physical layout, operating voltage and temperature ranges, time zero circuit yield, and the expected effects of long term degradation due to known failure mechanisms. Although these relationships can be studied using simple circuits, there may be integration effects which make it necessary to test specific VLSI products. Timely testing techniques are also needed to identify the set of most critical circuit paths which actually limit circuit performance and which should be fixed in a revision to improve performance.

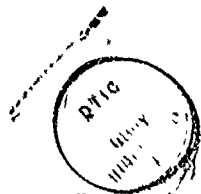
This project was undertaken to further develop a non-contact, laser photocurrent injection technique for obtaining information about timing margins at internal nodes of CMOS circuits. Conventional techniques used to obtain this information include computer simulations, contacting die probing, and electron beam voltage contrast waveform measurements. The laser technique described here has potential advantages over all of the conventional techniques, especially with regard to total equipment cost and possibilities for automation.

Initial work done in-house at RADC/RBRP reduced the basic concept to practice, but did not carefully model and measure the effects of photogeneration and collection on measurable device characteristics in both simple and complex circuits. One goal of this study was a fuller understanding of the expected behavior of simple CMOS gates operating under conditions of controlled photocurrent injection. Another goal was to further develop methods for obtaining timing margin measurements from many nodes of VLSI devices.

A PC based test bed incorporating a laser, Bragg cell modulator, and special device testing control was designed and used for this work. The effects of illumination on simple inverter performance were modelled and tested. Relatively large geometries limited the amount of timing delay which could be introduced at high V_{dd} voltages, but measurements at low V_{dd} were shown to agree with the models. These models can be used to predict the range of timing delay which can be introduced in smaller geometry devices.

Some unexpected difficulties were encountered during the tests on the microprocessor device, including noise in the laser modulator and in the measurement of maximum operating frequency. Although these were mainly due to equipment limitations, there were indications that dynamic device temperature patterns (possibly influenced by test sequence details), as well as device latch-up (particularly with high illumination levels at robust nodes) must be dealt with in a practical system. In some cases, it was noted that latch-up behavior was accompanied by permanent degradation of maximum operating frequency, but time constraints prevented a careful study of the reasons for this effect. It would be very desirable to automate beam placement by using design layout information. We remain interested in supporting further development and application of this, and other, device analysis techniques.

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 Project Engineer
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1 Introduction

1.1 Overview

An integrated circuit consisting of even a few digital gates may require several test sequences to fully characterize the chip, and as the chip complexity increases, the amount, and complexity of testing increases still further.

These complex tests consist of several aspects. One such aspect is state testing, where the chip is tested for proper functionality, given all digital input scenarios. Another is dynamic functionality testing, where the speed performance of a chip is tested, and various gates within are modified to optimize total chip performance. A third test is performance given certain supply and input voltage scenarios. For some logic families, such as TTL, with its narrow voltage definitions, this test is trivial. But for other logic families, such as CMOS, such testing can reveal weakness in the chip design in the same way that the second test for speed does. Also in the case of CMOS, the devices tested at very high or low voltages may be placed into normal operation at such voltages; and thus require testing at these voltages for device acceptance.

All test methods above may benefit greatly from die probing. Die probing is a method of generating currents or recording voltages at points within a chip, not limited merely to the external connections to the device. Die probing can isolate various circuits on a chip, with each circuit subjected to a simple test. Thus a complex test of an entire chip can be reduced to several simple tests specific to isolated circuits on a chip. Also, certain aspects of a chip can be uncovered and understood, that could not be, if the tests operated only on the chip's external connections.

Two techniques exist for probing an integrated circuit. The first method is contact die probing. In this method, a physical probe is aligned to contact a node within the integrated circuit. A voltage or current can then be injected or measured. This technique does not find favor among test engineers, as it is a destructive test technique. A special protective layer, called a

passivation layer, must be removed at the risk of destroying the chip, in order for the probe to contact the circuitry on the chip. The probe itself can also damage circuitry by destroying the metal contacts between circuit elements. CMOS devices are even more susceptible to damage of this type than TTL devices because of more critical device geometries.

The second technique, favored by test engineers, is called contactless die probing. This technique uses a laser beam or other illumination sources to generate currents within a chip. These currents, which are generated internally, can then affect operation within a chip in the same way that the currents injected by a contact probe do. One advantage of this technique is that the passivation layer need not be removed, as it is transparent to the laser beam. Also, the mechanics for placing a laser beam are simpler, and do not destroy the circuitry in its operation. The only disadvantage is that the voltages inside the chip cannot be measured directly, rather, all measurements must be on the external connections, and only on the basis that a circuit failed or not. However, circuit subsections still can be isolated using this technique, with corresponding test procedure simplification.

The contactless die probing technique can assist in the three test aspects (logic, voltage, and timing). Several companies are investigating the use of contactless probing to assist in logic state testing. This report presents the results of a study on the effects of injection current on CMOS inverter performance.

The CMOS inverter is the basic cell of a CMOS integrated circuit. Knowledge of CMOS inverter behavior undergoing illumination can be used to deduce illuminated behavior of a more complex device.

Using the results of work carried out on a simple CMOS device, a contactless technique has been developed which uses the charge carrier generation ability of a laser to measure timing margins in CMOS signal paths.

The technique has advantages over existing contactless techniques. It is less expensive than SEM electron beam techniques to implement and maintain. Probing does not occur in an inconvenient vacuum environment, and the charge build up problems associated with electron beams do not occur (Shiragasawa, et al. 1985). Further, it is not as destructive as electron beam scanning. The technique also has some drawbacks. The technique can only induce currents, and responses to the probing are measured only at the standard output pins of the test device. This limits the range of applications of the technique.

Logic state extraction, latch-up sensitivity, and device imaging are documented uses of laser probing. Now, using laser photocurrent injection and large signal MOSFET behavior curves, a procedure has been developed to measure the timing margin of signal paths in a complex CMOS device.

In the procedure, charge carriers are generated in the depletion region surrounding the drain of a transistor in a CMOS logic gate. These carriers will induce a current between the output load capacitance and the substrate surrounding the drain if there is a voltage difference between the load and the substrate. This current will either increase or decrease the propagation delay of the logic gate. The change in propagation delay is used in a test procedure in conjunction with MOSFET behavior models to determine signal path timing margins.

1.2 Description of Sections

This report presents the records of over a year of work and effort. The information is presented in a sectional form, with each section containing data as follows. Section one is the introduction. It introduces the concepts presented in this report. Section one also contains this introduction.

Section two presents the concepts and phenomenon that were applied in this research. Carrier generation, Photocurrent Injection, and CMOS logic gate behavior is reviewed.

Section three covers the simulations carried out during this research. First, the simulations carried out during the simple device study is presented. This includes SPICE simulations of inverter behavior, large signal MOSFET equation simulation, and a simulation of the simple device test. The second section covers the simulation and modeling conducted in conjunction with the complex device study. This includes a regressive analysis and a simulation of the experiment.

Section four details the simple device test experimental procedure, and section five covers the complex device test experimental procedure. These sections also cover the experimental set up for their respective tests.

Section six is the final section, and provides concluding remarks. The outcome and results of the simple device study are reviewed, and the outcome and industrial feasibility of the complex device study are reviewed.

This report has six appendixes. Appendix I contains the test code and test results of the simple device test. Appendix II contains the test vector for the complex device test. Appendix III contains the results of the node ranking experiments of the complex device test. Appendix IV contains the results of the state ranking experiments of the complex device test. Appendix five contains results of one series of simulation runs of the complex device test in which the criticality indicators were examined. Appendix VI contains a theory of operation of the test electronics, and Appendix VII contains the schematics of the test electronics.

The Appendices are available on a request basis from Rome Air Development Center. Contact Daniel Burns, RADC/RBRP for more details.

2 Concepts

2.1 Illumination on CMOS Inverter

Before we can qualitatively define photoinjection behavior of a CMOS inverter, we must first understand the behavior of the inverter in absence of photocurrent injection. The operation of a MOSFET and its behavior within the inverter circuit must be understood.

2.1.1 MOSFET Behavior

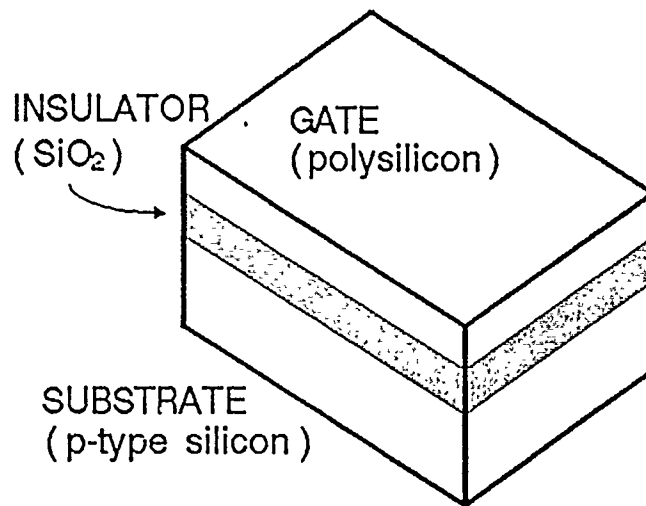
2.1.1.1 MOS Structure (MOS capacitor)

The MOS structure is a semiconductor that is doped so that an excess of electrons or holes are produced. On top of this, a thin layer of oxide is either deposited or grown to form a thin insulator. On top of this oxide, a layer of metal or polysilicon is deposited, as shown in Figure 1a. The semiconductor is called the substrate, and the metal is called the gate. For the following example, the semiconductor is assumed to be p-doped (excess holes). When the gate is disconnected, with no electric field within the oxide, the carrier distribution within the substrate is constant.

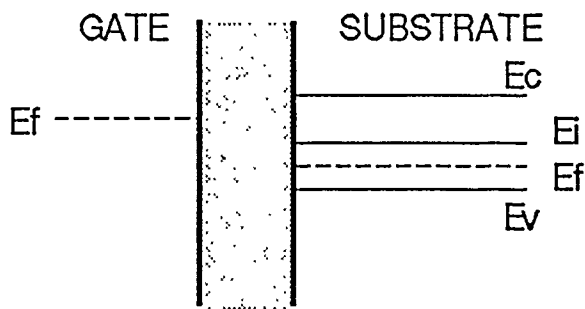
Let the gate potential now be lower than the substrate potential (negative gate voltage). As shown in Figure 1b, the holes in the substrate will tend to accumulate toward the negatively biased gate. This mode of operation is the accumulation mode. This mode does not have much use.

Let us raise the gate potential, so that it is positive with respect to the substrate potential, as in Figure 1c. The holes will now be repelled from the gate structure, and a region will be formed that is absent of any carriers, called the depletion region. This mode of operation is called the depletion mode and also finds little use.

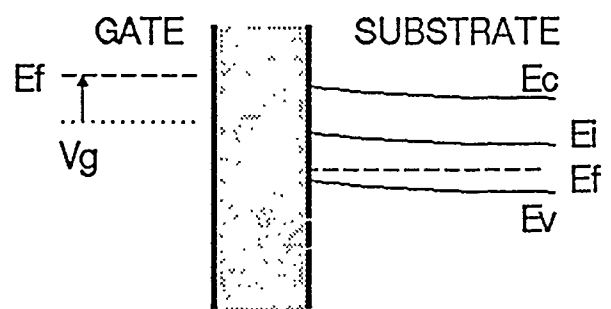
Let us further raise the gate voltage, so that the electric field in the gate structure is powerful enough to attract electrons from within the substrate, as in Figure 1d. This forms a thin channel that can conduct current with opposite charge of the normal carrier type within the substrate. This inverted charge is what gives this mode of operation the name: inversion mode. This mode is the normal current conducting operating mode within a MOSFET, with the inverted charge concentration forming a channel in which current can flow. The voltage between the gate and the substrate when this channel begins to be formed, is called the threshold voltage.



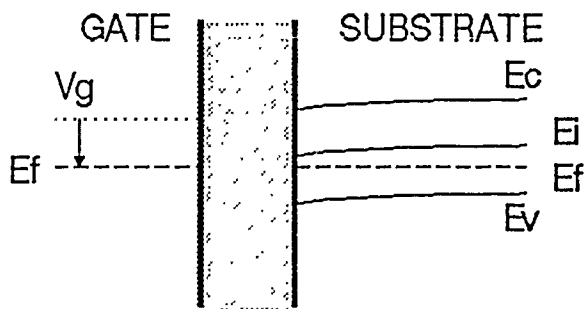
Physical Layout



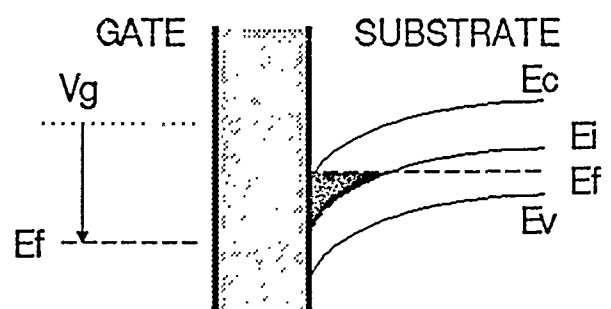
1a Flat Band Energies



1b Accumulation Operation



1c Depletion Operation



1d Inversion Operation

Figure 1 MOS structure and band energies for various biases.

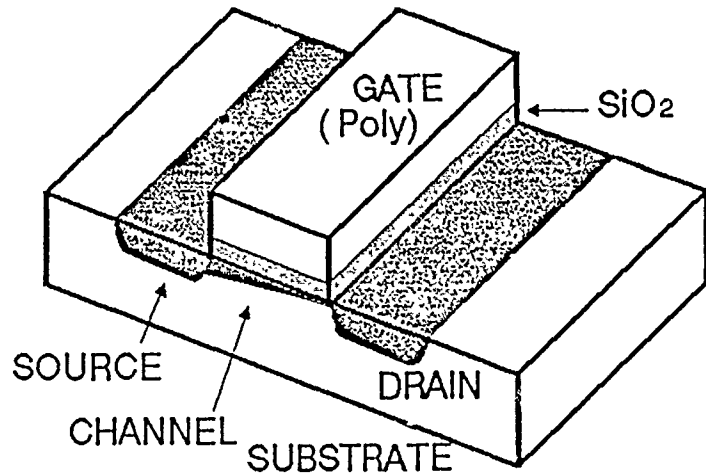
2.1.1.2 MOSFET Structure

Now let us form two regions with the same polarity as the inversion layer polarity (Figure 2a). These regions are placed on opposite sides of the gate structure. These regions are formed by doping the desired locations, so that an excess of opposite carriers, with respect to the substrate, is produced. For the example above, this doping would produce an excess of electrons. Two p-n diodes are formed with depletion regions at the junctions of these two doping regions. Under normal operation, but with no inversion channel, the two diodes that the regions create are connected back-to-back and do not conduct current. Let one of these regions be called the source and the other be called the drain. The naming for the gate and substrate remain unchanged. Also let the source be electrically connected to the substrate and be connected to the most negative point in an external circuit. (Only for our p-substrate transistor. For an n-substrate transistor, the source would be connected to the most positive point.) Let the drain potential be more positive than the source potential, so as to reverse bias the diode formed at the drain region.

If the inversion layer under the gate does not exist, then no current will conduct from the source to drain. As the gate potential is raised past the threshold voltage, and

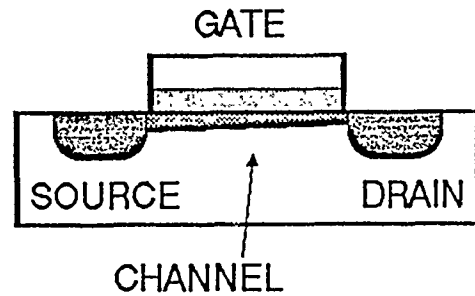
an inversion layer is formed, current will begin to conduct between the source and drain areas, as the material between now has the same characteristic charge concentration as the source and drain regions (Figure 2b). If the gate potential is further raised, the channel will widen, with resultant increase in current. Thus, this transistor is capable of amplifier action.

The transistor in our example has a channel formed by electrons, and therefore, is called an n-channel transistor. A transistor with holes is called a p-channel transistor. This convention of naming transistors will be used throughout this paper.

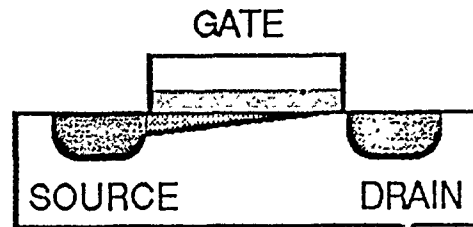


2a Structure of MOSFET with inversion channel.

2b
MOSFET in linear
operation region.



2c
MOSFET at edge of
operation in saturation
region.



2d
MOSFET in deep
saturation.

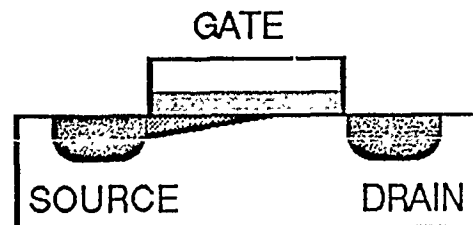


Figure 2 behavior of MOSFET channel

2.1.1.3 Modes of Operation

MOSFETs have two regions of operation. The first region is called the linear, or resistive region, which is characterized by large channel forming gate voltages. Another region of operation occurs if the drain voltage is sufficient. The field between gate and drain at the drain will then be insufficient to sustain an electron channel near the drain. The remaining electron channel will be pinched off next to the drain region. An extremely narrow high velocity electron channel will result, that will grow in length as the drain voltage increases (Figures 2c and d). The channel no longer exists here, with the electrons being swept to the drain at a saturation velocity. A strong electric field in this area causes this. This behavior is characterized by a drain current that is independent of drain voltage, but is dependent on gate voltage. This region is called the saturation region. A plot of drain current versus drain voltage, with varying gate voltage, is shown in Figure 3, with linear and saturation regions marked.

If we assigned V_G to the gate voltage,

V_T to the threshold voltage, and

V_D to the drain voltage,

then $V_D = V_G - V_T$ is the point where this insufficient-field pinchoff condition would just occur. With $V_D < V_G - V_T$, the channel would be complete, and the transistor would operate in the linear region. If $V_D > V_G - V_T$, the channel would be further pinched off, and the transistor would be operating in the saturation region.

2.1.1.4 Drain Current Calculation

For this paper, we are most interested in the application of the MOSFET in a CMOS inverter. Suffice it to say that there are several equations that relate the drain current to the gate voltage. All of the equations to be mentioned have been solved using the continuity equation and by applying certain boundary

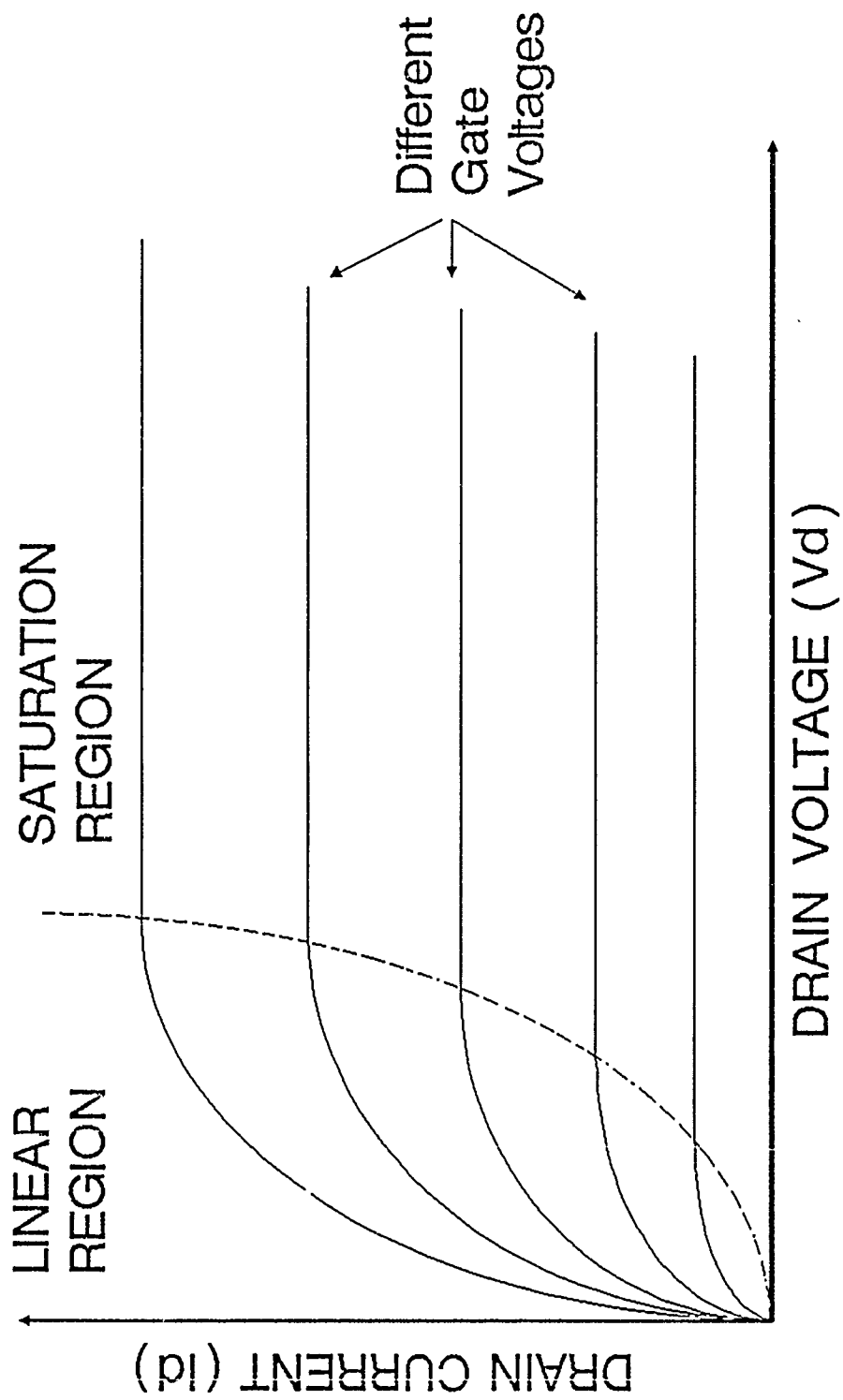


Figure 3 Output Characteristics

conditions. One boundary condition is the channel profile with respect to distance from source to drain. Figure 2c and d imply that this profile is linearly variable. This is not the case, but solutions to a nonlinear profile are very difficult, and normally follow some numerical algorithm. Making an assumption, that the profile is indeed linear, we get

$$I_D = \frac{\bar{\mu}_n W C_i}{L} \left\{ \left(V_G - V_{FB} - 2\phi_F - \frac{V_D}{2} \right) V_D - \frac{2}{3} \sqrt{\frac{2\epsilon_s q N_a}{C_i}} [(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}] \right\} \quad (1)$$

where I_D is the drain current,

$\bar{\mu}_n$ is the surface carrier mobility

(electrons, in this case),

W is the channel width,

C_i is the gate to channel capacitance,

L is the channel length,

V_G is the gate voltage,

V_{FB} is the flat-band threshold voltage,

ϕ_F is the metal-semiconductor work function
between the gate and substrate,

V_D is the drain voltage,

ϵ_s is the relative permittivity of
the silicon substrate,

and N_a is the approximate doping
concentration in the substrate.

The term $\bar{\mu}_n Z C_i / L$ is usually a process constant, and is normally given the name 2β . The terms V_{FB} and ϕ_F sum together to give an adjusted threshold voltage. In the above equation, the threshold voltage is not found easily, as the charges across the gate region, and therefore the field in the gate region changes with varying depletion charge, and thus changes with varying drain voltage. If we ignore these changes, the equation above then becomes

$$I_D = \frac{\bar{\mu}_n Z C_i}{L} \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right] \quad (2)$$

where V_T is the threshold voltage, as defined before.

The equation above is for the linear region. If V_D is substituted for $V_G - V_T$ then the above equation becomes

$$I_D = \frac{\bar{\mu}_n Z C_i}{2L} V_D^2 = \frac{\bar{\mu}_n Z C_i}{2L} (V_G - V_T)^2, \quad (3)$$

which is the equation for the MOSFET in the saturation region.

The two formulas above do not characterize the MOSFET as well as the first formula, but they lend themselves more easily to application oriented computation. These formulas are used in SPICE (the simulator used in this paper), and likewise will be used to calculate CMOS inverter behavior.

2.1.1.5 Empirical Estimation of V_T and β

The two equations (2) and (3) rewritten with β become

$$I_D = 2\beta \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right] \quad (4)$$

and

$$I_D = \beta (V_G - V_T)^2 \quad (5)$$

for the linear and saturation regions, respectively.

If a transistor within a CMOS inverter can be maintained in the saturation region for all gate voltages, then the terms, V_T and β , can be found by measurement. To find both, the inverter must be connected in the manner shown in Figure 4 and subjected to different gate voltages. The ammeter on the output will measure the drain current through the transistor opposite of the meter, while effectively disconnecting the transistor across the meter. In no case is the drain voltage V_D , which is fixed at 5

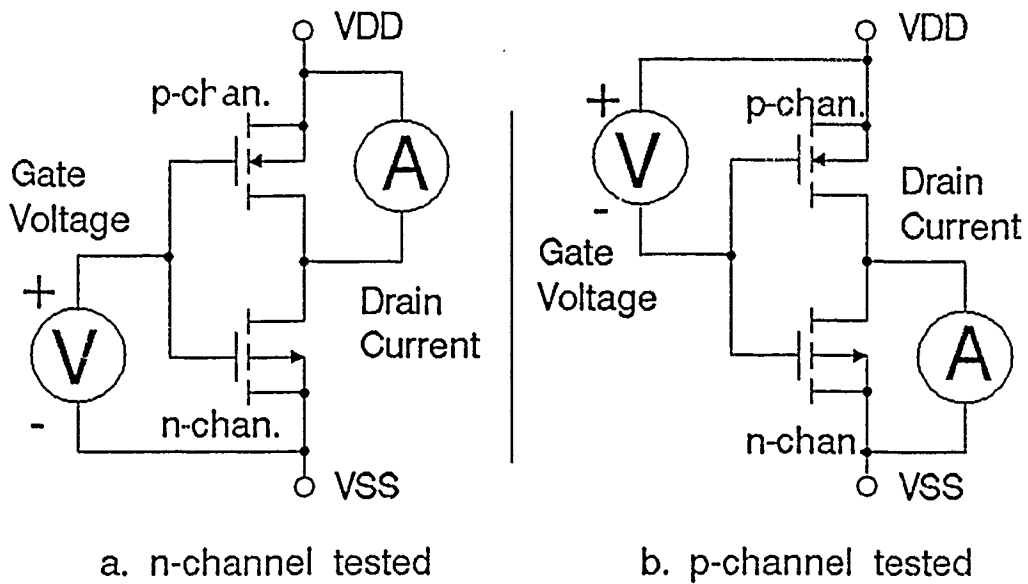


Figure 4 Testing gate voltage/drain current of MOSFETs in inverter.

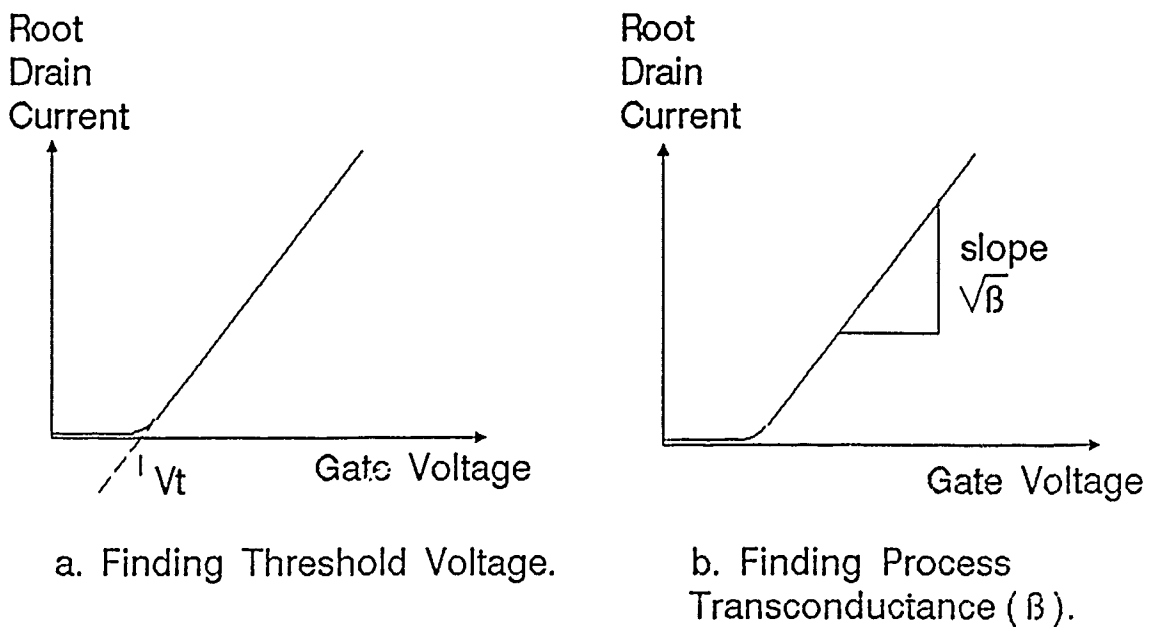


Figure 5 Determining threshold voltage and process β from gate voltage / drain current curves.

volts, allowed to be less than the linear region threshold $V_G - V_T$. Therefore, the transistor under test is always in the saturation region.

If the square root of the drain voltage is plotted versus gate voltage, then the threshold can be found by extrapolating the slope portion of the curve down to the V_G axis (mantissa). The voltage where the extrapolation intersects the V_G axis is then the threshold voltage, V_T . This procedure is shown in Figure 5a. Knowing the slope of the curve at the beginning of the extrapolation of V_T , which is also the slope of the extrapolation, one can find β . This slope is the square root of β . This procedure is shown in Figure 5b. For a 74HCU04AJ hex inverter chip, the transistors will have a V_G between .5 and 1 volt and a β of between .005 and .03 amps/volt².

2.1.2 CMOS Inverter Behavior

2.1.2.1 Inverter Circuit and Static Behavior

The CMOS inverter is composed of n- and p-channel transistors, so that their gates are connected together and to the input, and their drains are connected together and to the output. The n-channel source and accompanying substrate is connected to ground (0 volts), and the p-channel source and substrate are connected to the supply (+5 volts). Notice in Figure 6a that the p-channel transistor has an n-type substrate, and the n-channel transistor has a p-type substrate. The p-type substrate of the n-channel transistor is in the form of a well within the n-type substrate of the p-channel transistor. Actually, most designs of CMOS chips attempt to place as many of the n-channel transistors in a single well to minimize space requirements, as room is required between n- and p-channel transistors to minimize other processing and operation problems.

The inverter schematic is shown in Figure 6b and is the same as the transistor connections in Figures 4a and b. Let us suppose that the input voltage is zero (logic zero.) The n-channel transistor does not have sufficient gate voltage to turn on. (The

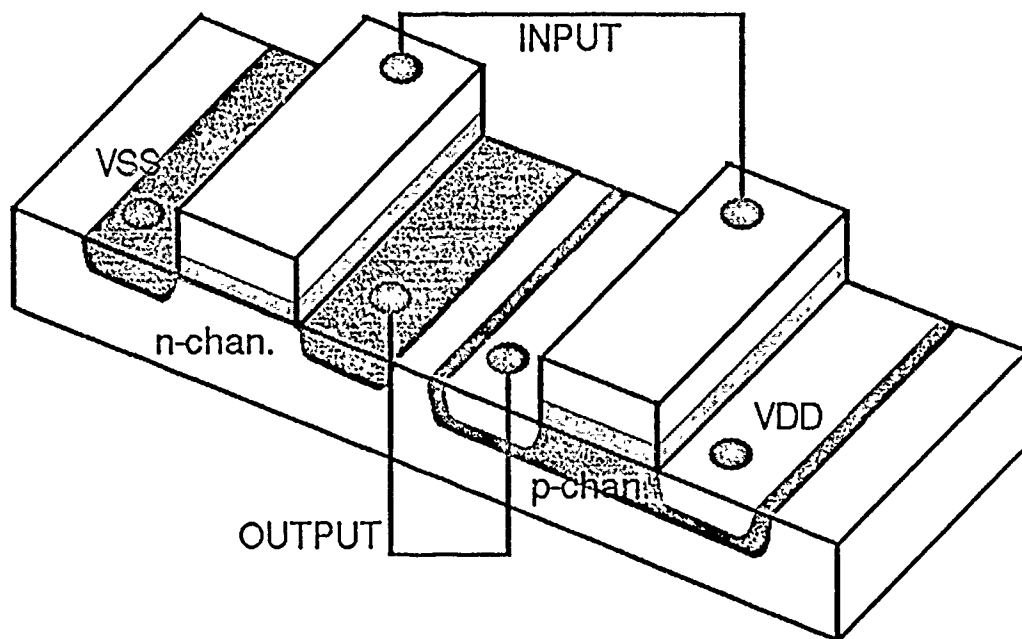


Figure 6a CMOS inverter layout.

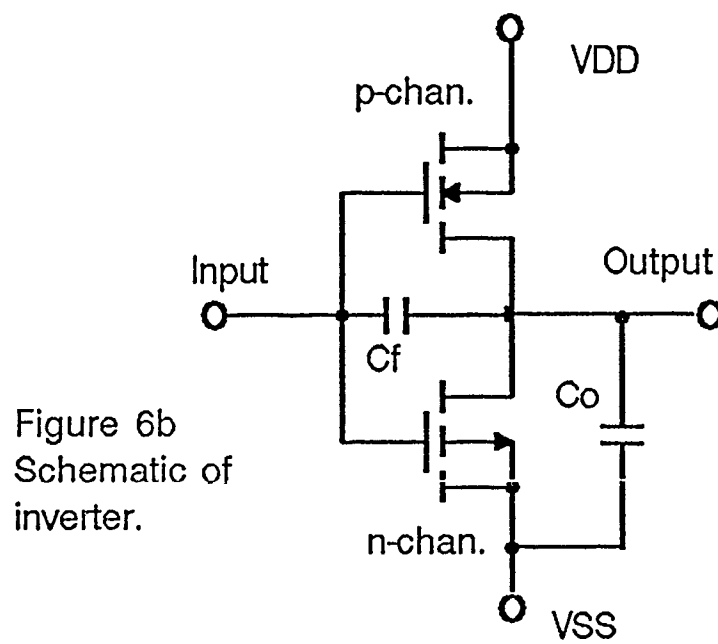


Figure 6b
Schematic of
inverter.

n-channel transistor does not have an inversion layer.) The p-channel transistor, however, has sufficient voltage to turn on, as its gate to source voltage is five volts. The output voltage is at five volts, because the p-channel transistor is connecting the output of the inverter to the supply, and the n-channel transistor is not conducting current to ground. Since the output is at five volts with the input at zero, then the circuit is properly functioning as the inverter. The same is true with the input at five volts, as the n-channel transistor is now conducting, the p-channel transistor is not conducting, and the output is zero. Figure 6b, however, has an added load capacitor and an added feedback capacitor to account for the speed performance of the inverter. (an appendix presents a method for measuring this capacitance.) Most of the propagation delay of a CMOS inverter is caused by a set of transistors that have high resistances charging a described load capacitance for a period of time. The process of charging and discharging this capacitance will be described using two different input conditions.

2.1.2.2 Dynamic Behavior

Instantaneous Input Signal Change. This method does not take into consideration input signal rise time. Analysis will proceed as if the output did not react to the input until the input has completed its transition. The gate signal in all of these computations is assumed to be constant. We will use the constant depletion mode approximation for all MOSFET behavior (equations 2 and 3).

Let us suppose that the output is five volts (logic high) and the input has completed rising to five volts. After a certain time (about 100 ps) when the carriers within the transistors have settled into a definite operation (a delay predicted by carrier movement theory) the n-channel transistor will begin to conduct. The output voltage will rise to above the supply voltage, providing current to discharge the feedback capacitor. The output will then begin to

drop in voltage as the feedback capacitor charges, and the output capacitor discharges through the n-channel transistor. The rate of discharge is constant (with a linear voltage slope) with the n-channel transistor in the saturation region until the output voltage drops below $5 - V_T$. When this occurs, the n-channel transistor transfers to the linear (resistive) region and the output signal begins to resemble an exponentially decaying curve. This curve continues until the output voltage has reached zero, which is the steady-state output voltage of the inverter with five volt input. Figure 7 shows the input and output curves of this behavior with the linear and saturation regions marked. The formula for finding the current charging a capacitor with known rate of voltage increase across that capacitor is

$$I_c(t) = C \frac{dV_c(t)}{dt}. \quad (6)$$

In this case, the voltage across the capacitor $V_c(t)$ is the drain voltage of the transistor, and the current charging the capacitor $I_c(t)$ is the drain current of the transistor. Equating (6) with (5) gives

$$C \frac{dV_D}{dt} = -\beta(V_c - V_T)^2 \quad (7)$$

which is the differential equation describing the output waveform when the transistor is in the saturation region. Applying the initial condition that at $t=0$, the output voltage V_D is the supply voltage + some positive voltage (0.7 volts for a p-channel transistor drain to substrate diode drop to compensate for the actions of C_F), the solution to the equation (7) above is

$$V_D = V_{supply} + 0.7 - \frac{\beta t}{C} (V_c - V_T)^2. \quad (8)$$

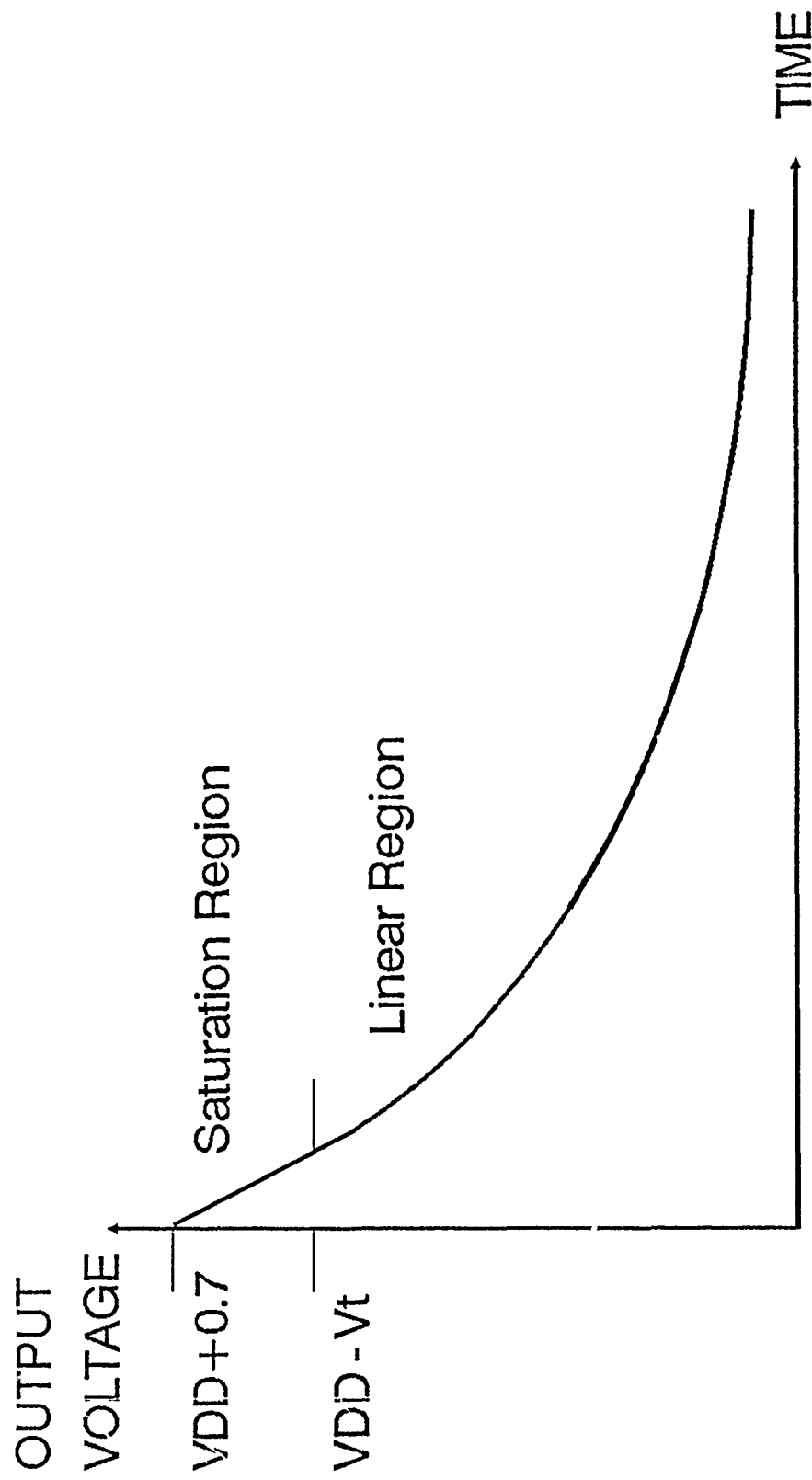


Figure 7 Transient output response
for two region model.
Instantaneously rising input.

This is an equation for a straight line with negative slope. The right side of (7) was nothing more than a constant. This equation is for the straight line portion of figure 7.

Doing the same for (4) gives

$$C \frac{dV_D}{dt} = -2\beta \left[(V_C - V_T)V_D - \frac{1}{2}V_D^2 \right], \quad (9)$$

which is the differential equation describing the output of the inverter when the transistor is in the linear region. The initial condition for this equation is that the output function be continuous at the linear-saturation boundary. The general solution to the above equation is

$$V_D = \frac{2A(V_C - V_T) \exp \left[\frac{-2\beta t(V_C - V_T)}{C} \right]}{1 + \exp \left[\frac{-2\beta t(V_C - V_T)}{C} \right]}, \quad (10)$$

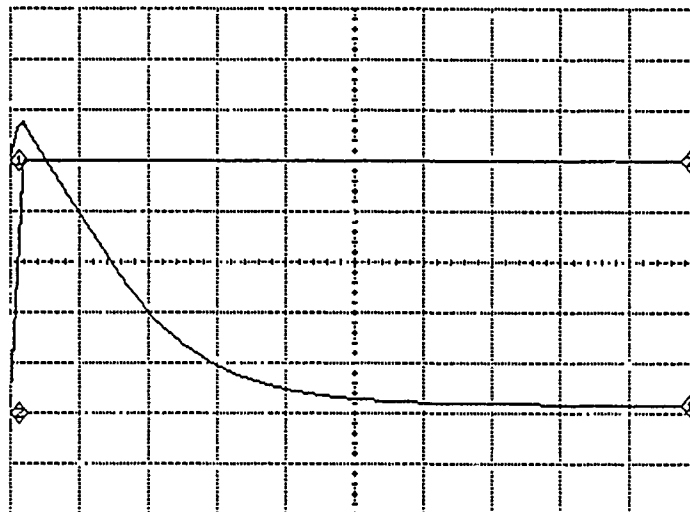
and is obtained by separation of variables, with partial fraction expansion to aid in solving the dV_D integral. The constant A is adjusted so that the two functions (8) and (10) are continuous across the linear-saturation boundary. (It actually so happens, that if $t=0$ at the onset of equation (10), A will be equal to 1.) These two functions are drawn to scale in Figure 7. They resemble a single exponential curve, and as such, may fit well with a simplified model of a single exponential. In chapter 3, such a model is developed.

Finite Time Input Change. The input signal of a real device will not be an instantaneous rise or fall, rather, it will be a ramp or exponential with finite rise time. The equations above are valid, given that V_C is variable with respect to time, and is the input voltage to the inverter. An additional term must be included in the above equations to account for the independent charging of C_i . Equations (7) and (9) then become second order differential equations. An example of an output characteristic with a finite time input is shown in Figure 8. The abscissa (X

coordinate) is time in 5 nanosecond divisions. The ordinate (Y axis) is inverter output voltage in 1 volt divisions.

PATH [.OUT] :
CINV

ANALYSIS TYPE
TRAN LINEAR



CHANNELS

CH 1 V(3)	TIME
YSCAL	1V/DIV
YZERO	3.86 V
XSCAL	5NSEC/DIV
XZERO	25.0NSEC
CH 2 V(1)	TIME
YSCAL	1V/DIV
YZERO	3.86 V
XSCAL	5NSEC/DIV
XZERO	25.0NSEC
CH 3	
YSCAL	
YZERO	
XSCAL	
XZERO	
CH 4	

Figure 8. Spice simulation of finite input characteristic.

2.1.3 Propagation Delay Definition and Measurement

The propagation delay of a CMOS inverter is the time from when the input of an inverter passes through half the supply voltage (2.5 volts) to when the output passes through half the supply voltage (also 2.5 volts in Figure 9). From a practical standpoint, during the time when the propagation delay is being measured, both the input and the output of the inverter are at the same value. The propagation delay may be well defined for the instantaneous input case where equation (10) passes through the $V_{supply}/2$ point, or it may lack such definition, such as in the case where the input signal rise time is longer than the inverter propagation delay. In this case, the second order differential equations that (7) and (9) become (under the section titled "Finite Time Input Change"), are used to find the propagation delay. It may be difficult to measure propagation delay in this case and compare meaningful

information to an accurate model. This is where hard assumptions and generalizations must be relied upon to give a representative model.

2.1.3.1 Model Assumptions

If the propagation delay is at least twice the rise time of the input signal, then the instantaneous input case may be used with a delay correction. This correction time begins when the input passes through the 50% supply voltage point. This is when the greater output current in the inverter is passed from one transistor to the other. The correction time ends when the counteraction current from both transistors into the feedback capacitor C_F exceeds the

current into C_F from the input voltage change, and therefore permits the output voltage to begin its transition. Before that, the sum current favors the input voltage change, which keeps the output at a diode drop above the supply voltage, as shown in Figure 7.

During this time, both transistors are in the saturation region, and behave according to Equation (5). The end of this correction time happens when the equation below is true.

$$C_F \frac{dV_{in}}{dt} = \beta_n (V_{in} - V_{Tn})^2 - \beta_p (V_{supply} - V_{in} - V_{Tp})^2 \quad (11)$$

where V_{in} is the input voltage,

β_n and β_p are the n- and

p-channel transistor betas, respectively,

and V_{Tn} and V_{Tp} are the n- and

p-channel transistor threshold voltages,

respectively.

This is not a differential equation to be solved in the usual sense. In this case, the input voltage and slope are known, and the time necessary to make this equation true is found. However, if one solves this equation in the general sense, the time can be found. This occurs when the equation solution and the actual input signal for that time are the same value

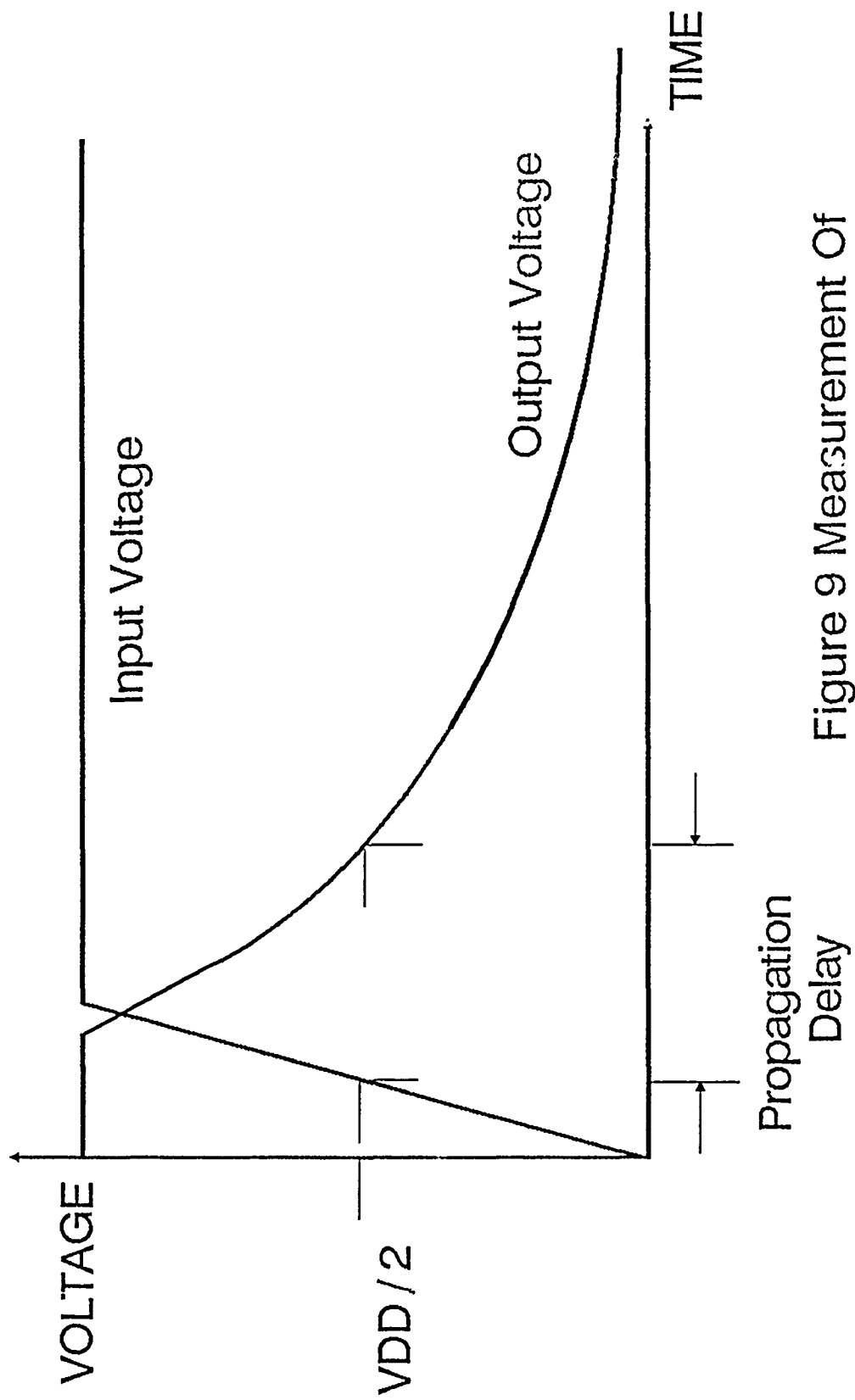


Figure 9 Measurement Of
Propagation Delay

and are within the confines of the supply voltages. For most cases, this time will be small with respect to the propagation delay.

The value C_F cannot be ignored when the inverter propagation delay is somewhat smaller than twice the input rise time. However, if the propagation delay is sufficient, only the saturation region of the output curve need be affected. If this is indeed the case, then only the first differential equation (7) is affected. If we make one further assumption, that the input signal is a linear slope rather than the normal exponential, then the modified (2.7), which is shown below

$$C_L \frac{dV_D}{dt} - C_F \frac{dV_{in}}{dt} = -\beta(V_{in} - V_T)^2 \quad (12)$$

reduces to a first order equation with linear solution,

$$V_D = V_{supply} + 0.7 + \frac{V_{in} C_F - \beta t (V_{in} - V_T)^2}{C_L + C_F} \quad (13)$$

This equation is then substituted in place of Equation (8). Equation (10) can then be used without any reference to the changing input voltage after the transistors enter the linear region. This is an additional correction that can be applied to the simplified model.

To conclude, using some simplifying assumptions and indicated corrections, the behavior of an inverter can be defined within reason, and without using second order differential equations in doing so. These models describe the performance of a CMOS inverter without illumination.

2.2 CMOS Inverter Behavior

2.2.1 Device Latchup

This section is presented to make the reader aware of what might happen to a CMOS circuit if it were illuminated. This phenomena manifests itself when a CMOS circuit is indiscriminately illuminated. The

result is the reduction of chip performance, and indeed this occurred to several chips, during test on complex devices. The only reason the simple device was spared was because during device layout, serious attention was paid to prevent latchup.

A cross section of a CMOS circuit is shown in Figure 10a with parasitic n-p-n and p-n-p bipolar transistors. The schematic of this "parasitic silicon controlled rectifier (SCR)" is shown in Figure 10b. The circuit operates as such: If a small bias should be present on either the n-p-n or p-n-p transistor, they will conduct, biasing the other transistor to conduct. When the other transistor conducts, it biases the first transistor to conduct, and so on, until both transistors have turned on fully. Only power supply

removal will reset this circuit. Notice that the top and bottom terminal of this circuit is connected to the power rails directly. When these transistors conduct fully, they present a direct short circuit across the power supply. This action will normally destroy the transistors and any metallization immediate to this area, thus rendering the CMOS device inoperative.

Illuminating this circuit improperly will have the same results. For instance, as in Figure 10c suppose that the beam strikes the area between the n substrate and the adjacent p well. This will place a leakage current source across the base-collector junction of the p-n-p transistor (Figure 10d), forward biasing it and causing the above mentioned race condition. Therefore it is important to have known control over the intensity and position of the light source, and know when it will cause latchup. Regretfully several chips must be destroyed to obtain this knowledge.

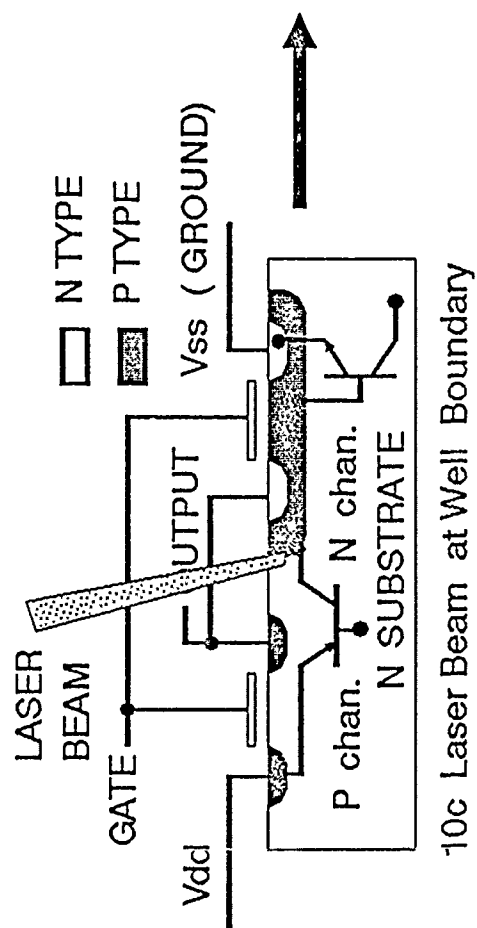
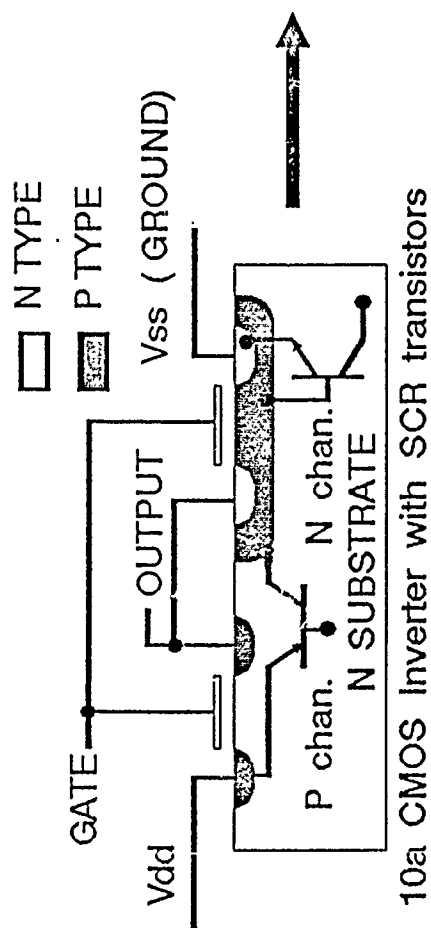
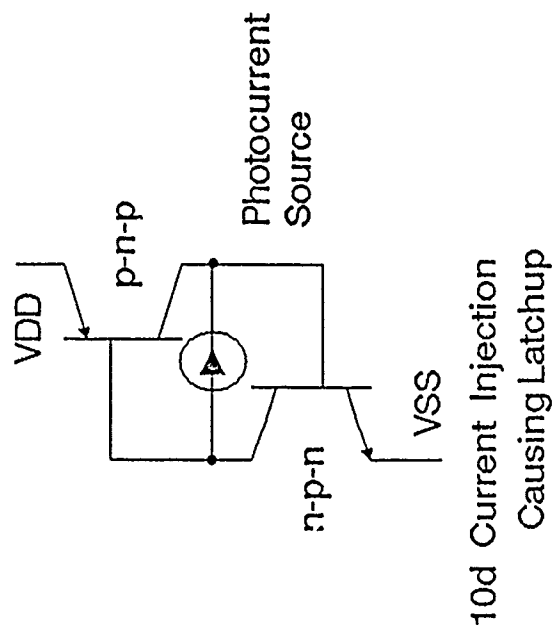
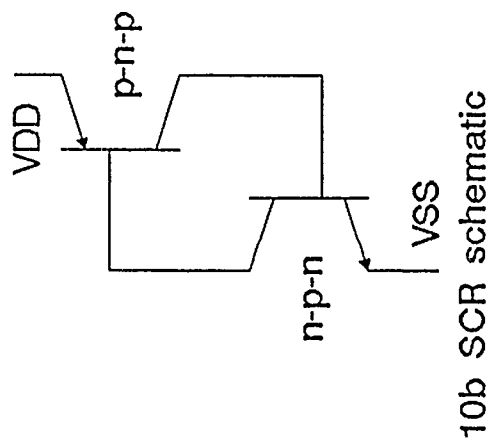


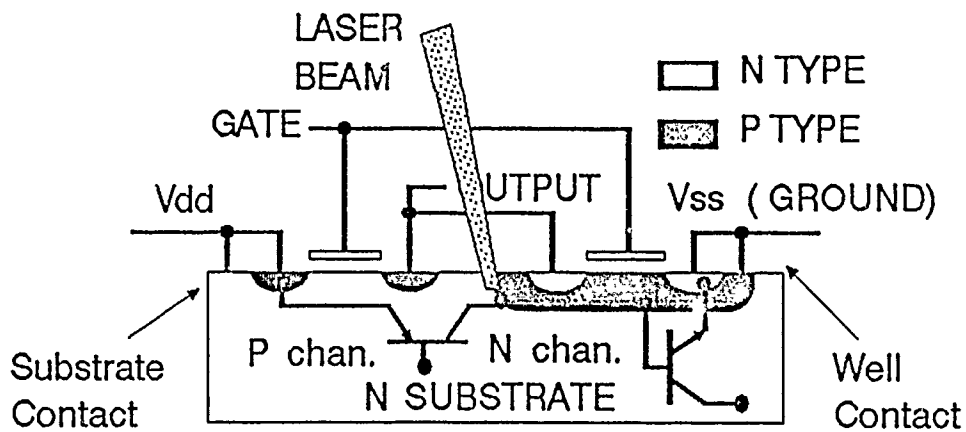
Figure 10 Latchup

There are methods to reduce occurrences of such latchups. It so happens, that the resistances between the base and emitters of these SCR transistors are rather high, and so it is easy to cause the transistors to conduct. One way of reducing these resistances, and at the same time reduce the current gains of the SCR transistors is to place low resistance contacts on the wells between the drain

contacts of the MOSFETs, and to connect them of the sources to the n- and p-channel MOSFETs, as shown in Figure 11a. The resistances between bases and emitters of the SCR transistors (Figure 11b) are now reduced considerably. Far more current is now required to initiate SCR action. For the simple device, no illumination could be generated to cause latchup. In interest of saving space, complex devices are constructed using procedures that are somewhat lax in totally preventing latchup, and so latchup might occur in complex devices.

2.2.2 Generation and Recombination

Carrier generation is the act of moving an electron from the filled valence band to the empty conduction band. The free electron in the otherwise empty conduction band can now contribute to current flow. The absence holes in the valence band also can contribute to current flow. Recombination is the act of filling one hole in the valence band with an electron in the conduction band. The missing electron and hole no longer contribute to current flow.



11a Laser Beam at Well Boundary.
VSS and VDD are connected to the well and substrate, respectively.

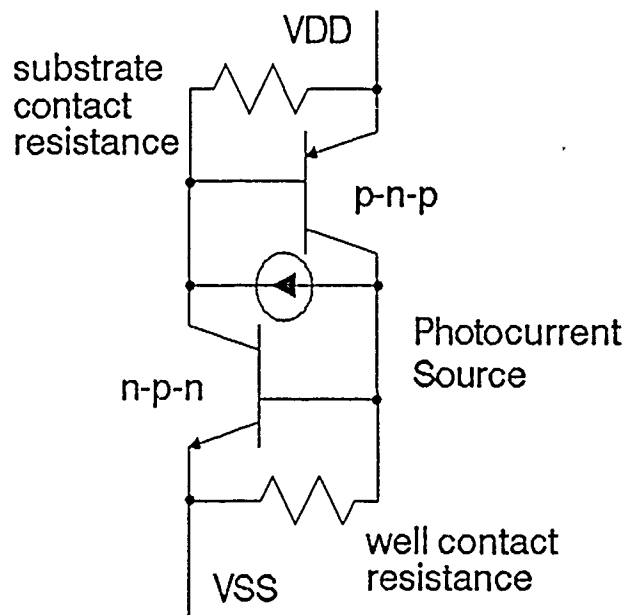


Figure 11b Photocurrent source has reduced effect on SCR transistor pair due to contact resistances.

2.2.2.1 Generation Methods

Three theorems are most widely accepted to account for generation and recombination. The first method is band-band generation. According to this method, the electrons in the filled valence band acquire enough energy through the absorption of a photon (light) to jump the band gap. The electron is then acquired into the empty conduction band. This jump does not involve changes in the crystal momentum, and therefore it is a purely direct jump. Direct semiconductors, such as gallium arsenide, are benefitted mostly by this. This is not the case, however, for silicon, as the photon energy of the laser used is about 1.4 eV, and the energy required for a direct vertical jump in the silicon band structure is about 3 eV.

The second method is band-band Auger (French pronunciation) generation. If an electron exists in the conduction band, and it has higher than the minimum possible potential, as a result of the conduction band being partially filled, then it can acquire another electron with a lower energy than the lowest energy in the conduction band. After interaction, both electrons would have similar energies with value between the two starting energies. Given an electron had a high initial energy in the conduction band, the electron rising from the valence band would not need to jump the band completely. There are reasons why this method does not account for generation in these experiments, however. To retain electrons in the conduction band at such high energies would require that the conduction band be very much filled. This means that the material would be a very good conductor. Three reasons say that is not true. The first is that any thermal energies present in the material, for being exposed to ambient temperatures, are not sufficient to fill the conduction band to the level needed. The second is that any doping concentration strong enough to cause Auger generation would hinder MOSFET operation. Concentrations on the order of 10^{20} donors/cm³ are needed to cause band-band Auger generation whereas the most concentrated doping in the drain structures of CMOS devices under

investigation is 10^{17} donors/cm³. The third reason is that the drain area, for any drain potential, would have a strong enough electric field to sweep any carriers from the conduction band.

The third method of generation is Shockley-Reed-Hall generation. After the electron rises to the minimum required band gap, the crystal goes through a change in momentum to acclimate the electron to the conduction band. The generation of these carriers is helped by intermediate trapping centers located inside the band gap. The electron would rise directly in energy with the absorption of a photon, where it would be retained in such an intermediate state, until the crystal completed changing momentum. A phonon (heat) would be liberated and the electron would be acquired into the conduction band. This is one such scenario and several others also exist, but this method in general is the principal for generating carriers in all indirect semiconductors, such as silicon, and will be the principal method in generating carriers within the CMOS device under investigation.

Regardless of generation method, one photon will produce one electron. This says that the carrier generation rate is merely proportional to the incident photon rate.

2.2.2.2 Recombination Methods

All generation methods outlined above will also work in recombination, but in reverse. For example, in direct band recombination, an electron falls in the potential gap to the valence band and liberates a photon.

2.2.3 Semiconductor Diode

2.2.3.1 Basic Operation

When n- and p-type semiconductor join, the free electrons and holes in their respective materials will combine and leave their oppositely charged ions behind in the crystal structure. The electric field generated within the structure by the ions increases

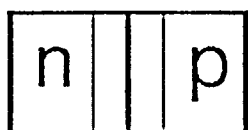
to match that generated by the free carriers. A region void of carriers is formed at the junction, called the depletion region. (Figure 12a) The Fermi level remains constant, however, the conduction and valence bands warp to accompany the junction, as in Figure 12b.

If the diode is reverse biased, as in Figure 13a, the band bending becomes more pronounced, with the Fermi level in line with the conduction and valence band bending. The valence band, filled with electrons from the external potential, cannot jump to the conduction band, made empty by the external supply, without help from photons (optical means) or an electric field large enough to penetrate the gap via states in the depletion region (avalanche). The diode, in a practical sense, is not conducting current.

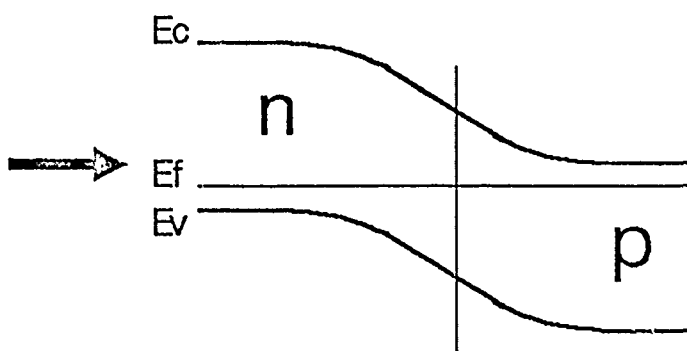
If the diode is forward biased past a certain threshold, then the Fermi level band bending is sufficient to cancel most of the p-n junction band bending and allow the electrons and holes to flow in their respective bands, as in Figure 14b. The diode conducts current freely, in a practical sense. Therefore, the diode can act as a one way current gate, allowing current in one direction, and blocking it in the other direction.

2.2.3.2 Photo Injection

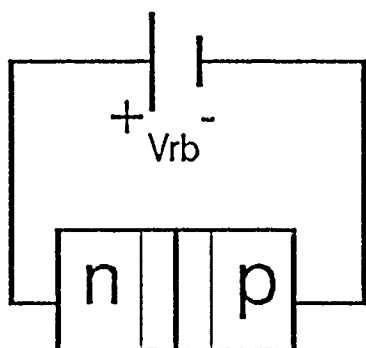
For this paper the discussion is centered on the photoinjection of a reverse biased diode. Many such junctions exist in CMOS devices, and photoinjection of any of these will generate the current necessary for CMOS experiments. In all of these reverse biased junctions, large depletion layers exist. Despite the fact that



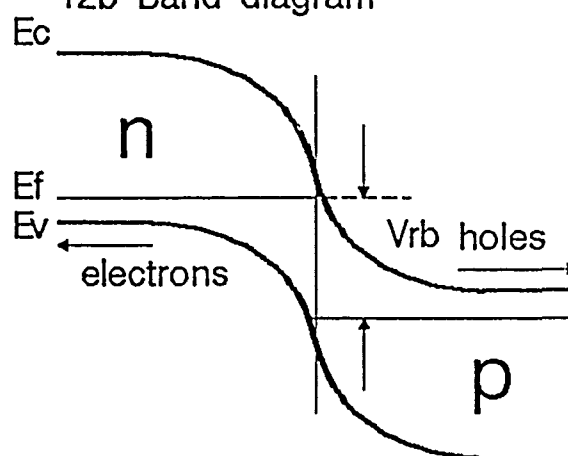
12a p-n junction



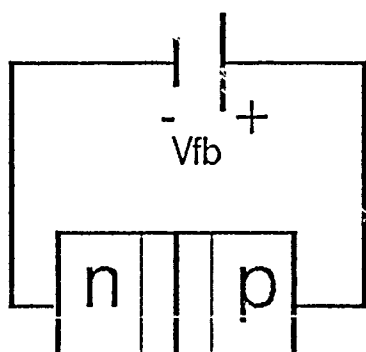
12b Band diagram



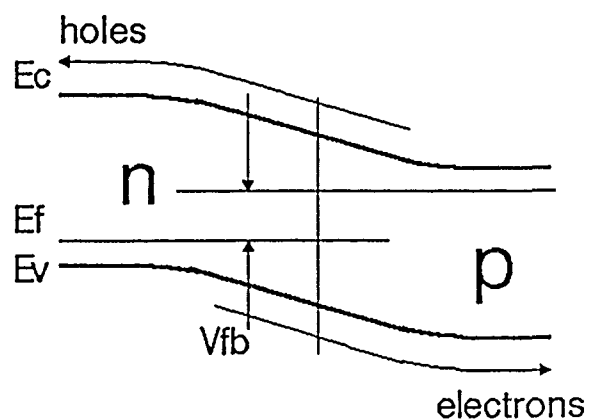
13a p-n junction
reverse biased



13b Band diagram. Notice
that carriers move away
from junction.



14a p-n junction
forward biased



14b Band diagram. Notice
that carriers move through
junction.

the depletion layer exists there, if the material is photoinjected at that point (Figure 15a), carriers will still be generated. However, the electric field at these depletion regions is sufficient to separate these carriers, and carry the electrons and holes to the n- and p-regions, respectively before they have a chance to recombine with each other, as in Figure 15b. Therefore, maximum useful carrier generation from photoinjection results when the light beam illuminates such a depletion region.

2.2.4 Optics on Substrate

The last section deals with the optical properties of the integrated circuit substrate. All of these properties introduce a constant intensity scaling factor. Figure 16 shows the cross section of a chip with a protection, or "passivation" layer on top. Light follows different paths with different outcomes. Most of these paths will have two factors per event, the first is reflection, and the second is absorption. The first factor (reflection) manifests itself in impedance (refractive index) differences between materials and off of metallization. They generate $e^{-\beta x}$ terms, which can be found using a Smith chart or programs to the like. The thickness of the passivation layer is important in this respect, as it transforms impedances between boundaries. The second factor is absorption.

A small number of photons are absorbed in the passivation layer (with their $e^{-\alpha x}$ terms, but a majority of absorbed photons generate electron-hole pairs within the silicon. Interactions, beyond the scope of this paper to describe, determine what percentage of absorbed photons that actually lead to generated carriers, but that percentage is rather good.

Some of this light is multiply reflected within the passivation layer. This "scattering" limits the useful size of a laser beam that can be used for a given intensity. For an exact spot of 2 microns, the scattering for bright beams can be anything between 5 and 20 microns.

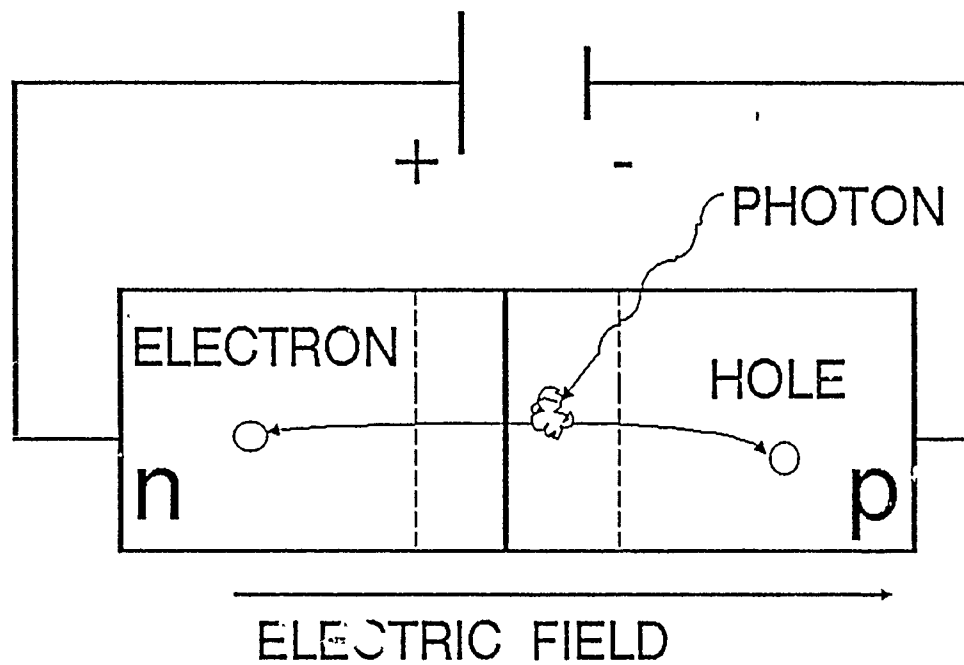


Figure 15a Electron - hole pair being generated.

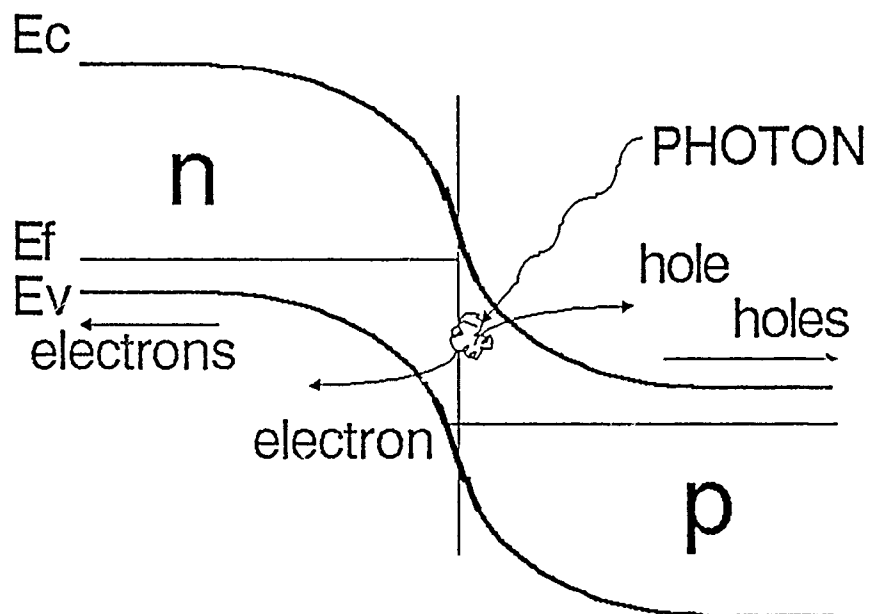


Figure 15b Band diagram with electron - hole generation introduced.

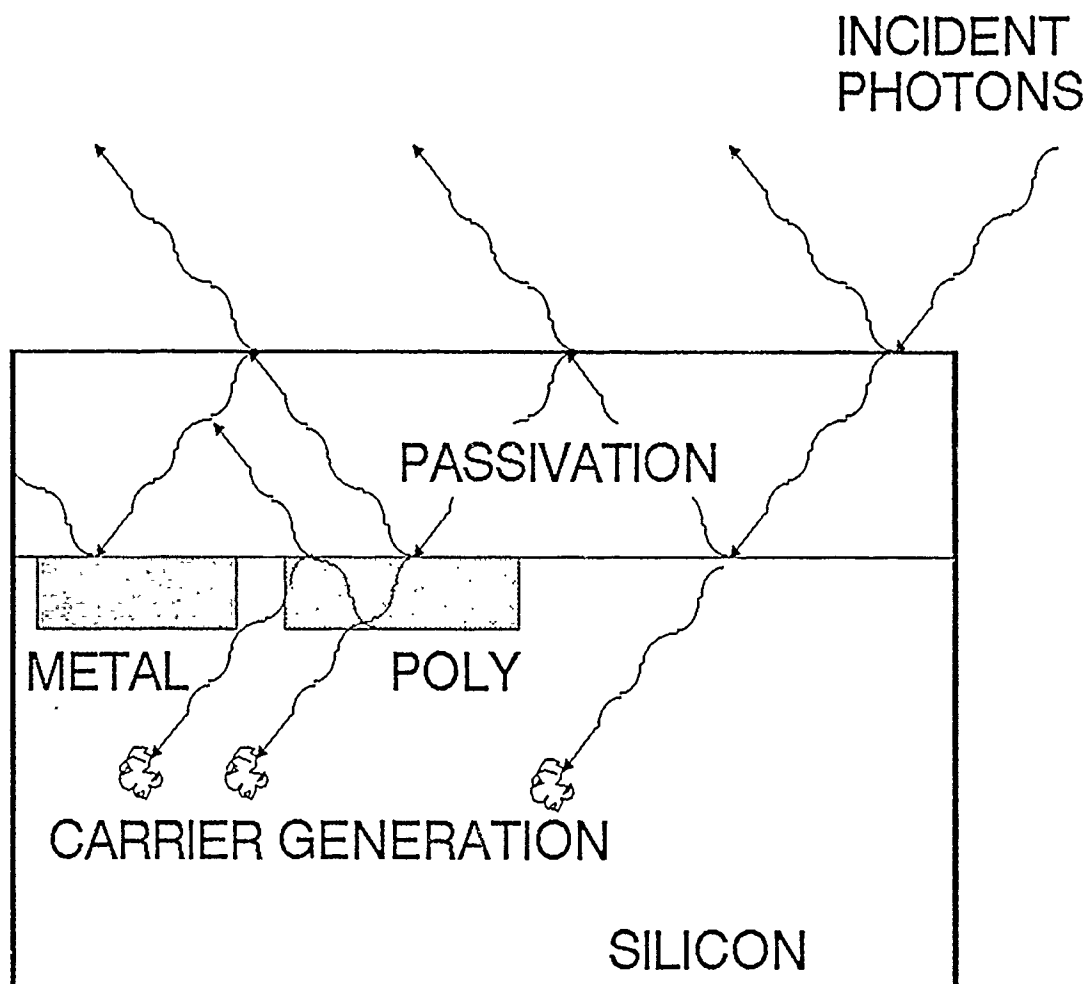


Figure 16 Light reflection, both internal and external limits the smallest spot size on the silicon. Notice the scattering.

The transfer function between illumination and carrier generation is linear, with the ratio of illumination and carrier generation being a constant. It is, as if the illumination was an input signal going through a linear attenuation, and then producing a proportionate number of carriers. All of the illumination currents discussed in the paper could very well be intensities scaled by a constant (with inverse meter²-volt units).

2.2.5 Inverter with Illumination

2.2.5.1 General

This section will now deal with the inverter in the presence of illumination. For the photocurrent injection to

be most effective, the drain areas of either the n- or p-channel transistors are illuminated. This will create a current source from the photogeneration carriers. If this light beam strikes the junction of the n-channel drain and well, as in Figure 17a, a current is generated. In effect, a current sink is created across the n-channel transistor, from the output to ground, as in Figure 17b. If the light strikes the junction of the p-channel drain and substrate, as in Figure 17c, then a current source is placed across the p-channel transistor, from the supply rail to the output, as in Figure 17d.

The photoinjection current, as it is generated mostly in the depletion region of a drain junction, will not change with drain voltage, but is instead dependent upon the timing and frequency of incident light.

2.2.5.2 Dynamic Behavior

We will now discuss the timing effects of illumination on the inverter. These equations follow the same pattern of development as the ones in section 2 for our negative output slope, n-channel conducting, instantaneous input case. The output curve of Figure 18, while not identical to Figure 7, has identical regions of operation to that of Figure 7. For the

instantaneous input case, the inverter first goes through operation in the saturation region of the conducting transistor. This behavior is a modification of (7) shown here with the current source added.

$$C \frac{dV_D}{dt} = I_{ILL} - \beta(V_G - V_T)^2 \quad (14)$$

I_{ILL} is the illumination current. A positive value of I_{ILL} will source current into the output and thus counteract the conducting n-channel transistor. A negative (sink) value will assist in n-channel conduction.

The current source modifies the slope of the output line when the inverter is in the saturation region. This only modifies the current present in equation (8), as shown below.

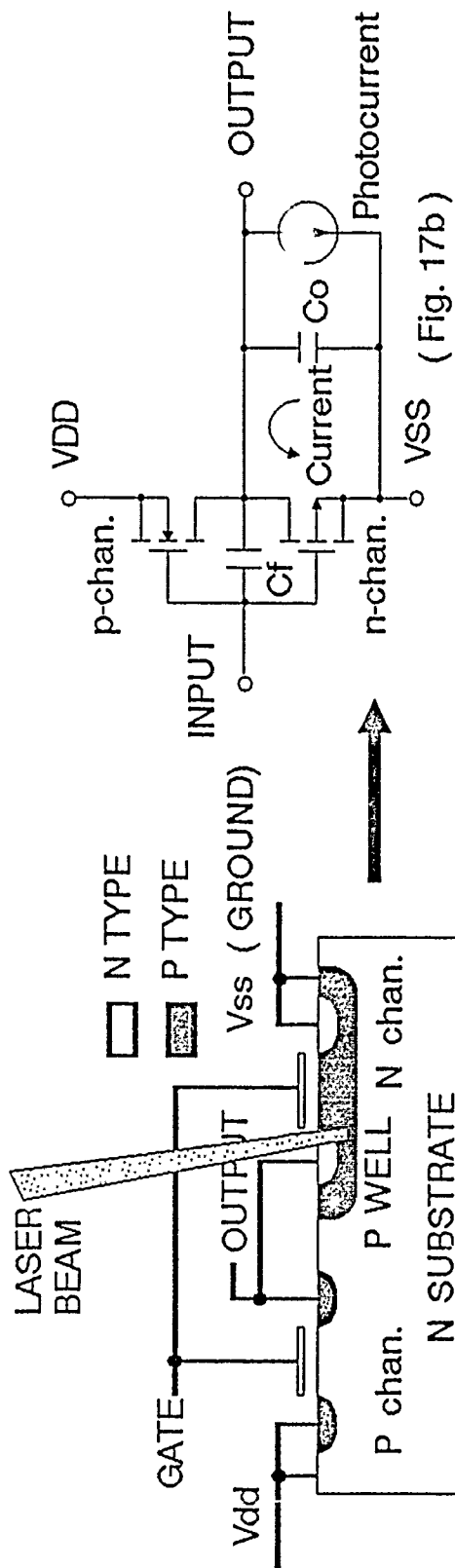
$$V_D = V_{supply} + 0.7 + \frac{t}{C} [I_{ILL} - \beta(V_G - V_T)^2] \quad (15)$$

A similar situation happens to equation (9) when the illumination modifies the characteristics of the linear region of Figure 18. The modified differential equation becomes

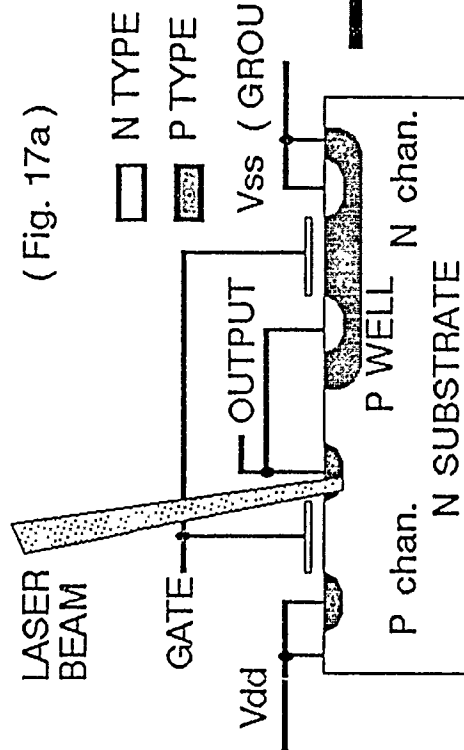
$$C \frac{dV_G}{dt} = I_{ILL} - 2\beta \left[(V_G - V_T)V_D - \frac{1}{2}V_D^2 \right]. \quad (16)$$

with solution

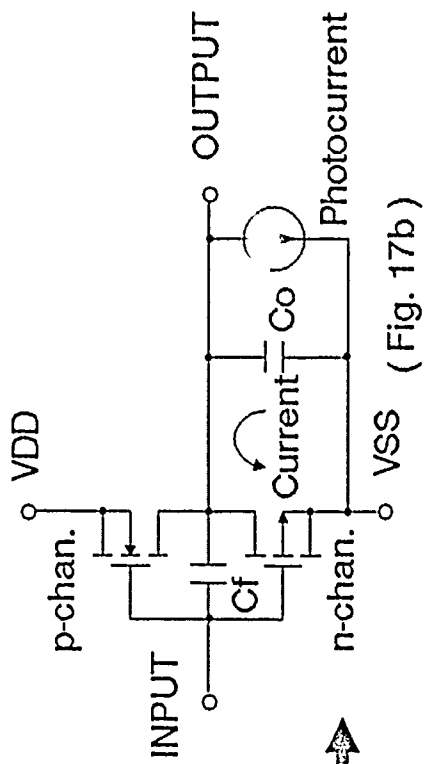
$$V_D = \frac{A \left[2\beta(V_G - V_T)(1 + e^{-k_1 t/C}) - k_1(1 - e^{-k_1 t/C}) \right]}{2\beta(1 + e^{-k_1 t/C})}, \quad (17)$$



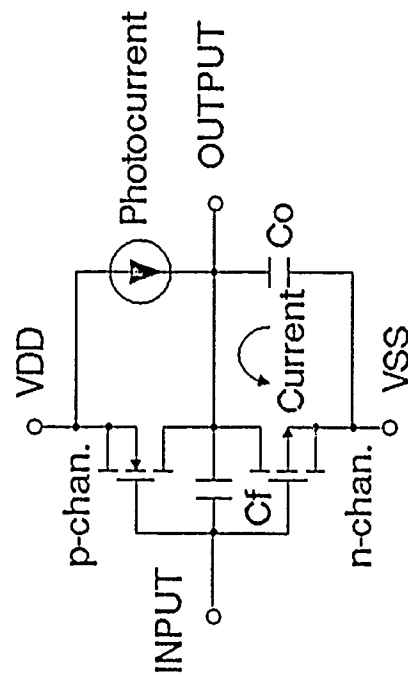
(Fig. 17a)



(Fig. 17c)



(Fig. 17b)



(Fig. 17d)

Figure 17 Photoinjection of n- and p-channel transistors with equivalent currents generated.

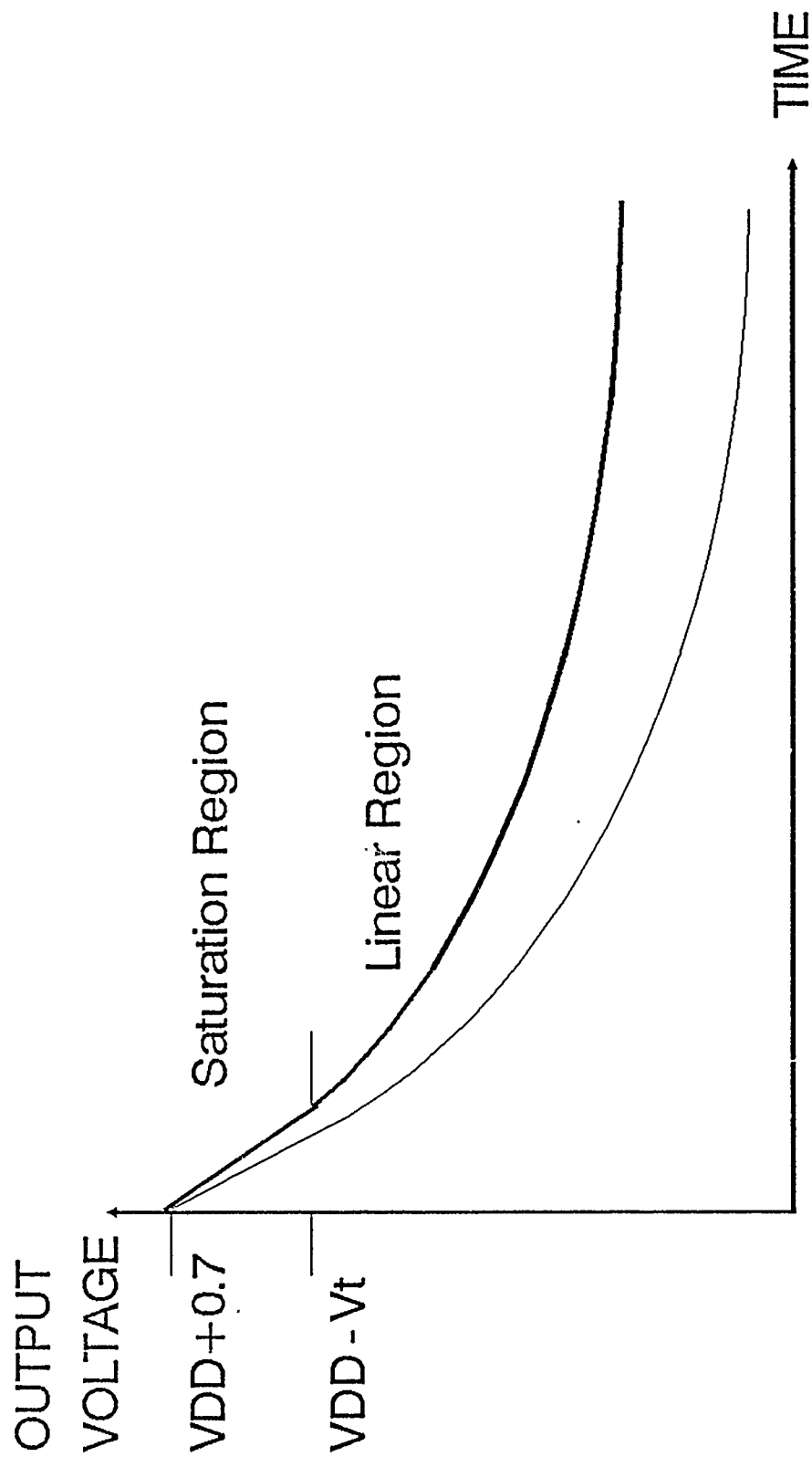


Figure 18 Transient output response for two region model using instantaneously rising input and subjected to photoinjection.

Where

$$k_1 = 2\sqrt{\beta^2(V_G - V_T)^2 - \beta I_{ILL}}$$

Equation (17) above reduces to (10) when I_{ILL} is set to zero.

There exists a limiting case to this equation, where $I_{ILL} > \beta(V_G - V_T)^2$. For (15), this case generates a positive linear slope, which owing to the power supply limitations, is equivalent to maintaining the output at the positive supply. For (17), this case generates an imaginary k_1 . For both equations, the physical significance is that the illumination current source totally overwhelms the conducting transistor, and completely prevents the input from affecting the output.

All of the techniques that were used in chapter 2 also apply to the above. Propagation delay is still measured at half supply voltage points, and as such, the above equations can be equated to $V_{supply}/2$ to find the propagation delay. The input delay correction equation (11) is modified as shown below

$$C_F \frac{dV_{in}}{dt} = \beta_n(V_{in} - V_{Tn})^2 - \beta_p(V_{supply} - V_{in} - V_{Tp})^2 - I_{ILL} \quad (18)$$

and is applied the same as (11). Corrections for the saturation region (Eq. 12 and 13) are modified to include the illumination current, so that (12) becomes

$$C_L \frac{dV_D}{dt} - C_F \frac{dV_{in}}{dt} = I_{ILL} - \beta(V_{in} - V_T)^2, \quad (19)$$

and (13) becomes

$$V_D = V_{supply} + 0.7 + \frac{V_{in} C_F + I_{ILL} t - \beta t (V_{in} - V_T)^2}{C_L + C_F}. \quad (20)$$

Equation 16 (modified equation 9) becomes a second order equation, as before, if any input condition other than a constant is used. Equation (19) and (20) rely on the input signal to be a straight line slope function.

2.2.6 Major Simplifications

2.2.6.1 Assumptions

This section discusses major simplifications. While the simplifications above attempt to preserve the theoretical model as much as possible, the ones presented below do not make that claim, rather they attempt to present some means of simply modelling data in an empirical manner. However, some tie to the theoretical model is assumed, and that is where we begin simplifications.

Notice in Figure 7 and Figure 18 that the curves roughly resemble a decaying exponential shape. One may go so far as to say that the saturation region models (which are straight lines) are part of this exponential curve. If this assumption is at all accurate, then a model can be derived that can simply describe inverter behavior. If we define a constant α so that

$$\alpha = \frac{2\beta(V_G - V_T)}{C},$$

for the instantaneous case, Equation (8) becomes

$$V_D = V_{supply} + 0.7 - \frac{\alpha}{2}(V_G - V_T)t, \quad (21)$$

and equation (10) becomes

$$V_D = \frac{2A(V_G - V_T)e^{-\alpha t}}{1 + e^{-\alpha t}} \quad (22)$$

with the instantaneous input case and the delay correction of equation (11). Now if we set $t=0$ at the point where the output begins to move, then the two functions can be approximated by

$$V_D = (V_{supply} + 0.7)e^{-\alpha t} \quad (23)$$

This model assumes that there exists no saturation region in which the inverter operates. This relieves the equation of the burden of having to deal with the straight line at the onset of an output transition. The output resistance of the transistor is assumed to

be constant, so that the multiple exponential solutions reduce to that of a single exponential. This is a most blatant assumption, but for these purposes, it is necessary.

It is left up to chapter four to give any merit to this assumption. No attempt will be made to prove its validity until the characteristic output curves (as in Figures 7 and 18) of all models and simulations are compared.

A further simplification can be made if the time required for the inverter output to go from $V_{supply} + 0.7$ to V_{supply} were separated from the main formula and included in the time calculation of (11). We will give the name τ_{pad} to this combined time adjustment. If τ_{PD} is the name for the propagation delay, then the equation

$$\frac{1}{2} = e^{-\alpha(\tau_{PD} - \tau_{pad})} \quad (24)$$

is the equation for the propagation delay of an inverter without illumination, and is solved from (23).

To simplify the expressions (15) and (17), an extra exponential must be included in (24) to account for the non-zero final-state approximation. Using the same assumptions and parent technique, the solution for the output of the inverter with illumination is

$$\frac{1}{2} = e^{-\alpha(\tau_{PD} - \tau_{pad})} + \frac{I_{ILL} R_D}{V_{supply}} [1 - e^{-\alpha(\tau_{PD} - \tau_{pad})}] \quad (25)$$

with $R_D = 1/\alpha C$, which is the drain resistance of the transistor with given gate voltage.

2.2.6.2 Important Effects

One can get these effects using the rigorous equations, but these simplifications help in describing where and how these effects occur. If (25) was rewritten to find propagation delay,

$$\tau_{PD} = \tau_{pad} + \frac{1}{\alpha} \ln \left(\frac{V_{supply} R_D - I_{ILL}}{V_{supply} R_D / 2 - I_{ILL}} \right), \quad (26)$$

and I_{ILL} was made to approach $V_{supply} R_D / 2$, the fraction within the logarithm would grow, thus the right side of (26) gets larger. This increases propagation delay. If I_{ILL} is made negative, then (26) would get smaller. This decreases propagation delay. The proper operating range is when $I_{ILL} < V_{supply} R_D / 2$. When $I_{ILL} = V_{supply} R_D / 2$, a singularity exists in (26). This condition is actually the injection current preventing the inverter output from going through the half supply voltage point. This point is needed for propagation delay measurement. To the propagation delay measurement equipment, the inverter behaves as if it had never switched. The injection current needed to obtain this "lockout" is

$$I_{ILL} = \frac{V_{supply} R_D}{2} = \frac{V_{supply}}{2\alpha C}. \quad (27)$$

Another singularity of opposite polarity exists when $I_{ILL} = V_{supply} R_D$. This occurs when the injection current is powerful enough to totally stop output action, and is also discussed with equations (15) and (17) as their limiting case. For propagation delay measurements, however, this singularity has no added significance.

These singularities do not have much significance in the simple device test, except to indicate where they are when an inverter output is totally locked. The simple device tests did not reveal these singularities, as the laser was not powerful enough to cause such a situation. However tests show that this case does indeed exist in the complex device, where geometries are rather small and low illumination intensities can disrupt a circuit.

This concludes the theoretical portion of this paper. The next two chapters will deal with proving this and the previous chapters.

2.3 Complex CMOS Device Behavior

2.3.1 Timing Margin Description

As this is an experiment designed to measure timing margin, it is necessary to define timing margin. In a complex device, signal paths are presented with logical values at clock transitions. The signal propagates through the logic in a finite time, and is then presented to the next signal path at the next active clock transition. Timing margin is the time after a signal has propagated through the logic in a path and before the active clock transition that requires the output of that path. With laser photocurrent injection, the propagation delay of a signal path may be increased, with a corresponding decrease in the timing margin of that path. Logic failures occur when this timing margin is reduced to zero.

In clocked circuits, several gates in a signal path are typically required to propagate a signal prior to the next clock edge. In this instance, the timing margin corresponds to the difference in time between the clock period (or some fraction thereof based upon the duty cycle) and the propagation delays in the signal path.

The propagation delay, and therefore the timing margin, can be modulated by injecting charge carriers at the drain of one of the logical gate transistors. This creates an additional current that moves charge either into or out of the output load and will either increase or decrease the propagation delay. This current is proportional to the incident laser beam intensity, and so can be modulated by modulating the intensity of the beam. Only the instances where the propagation delay is being increased are useful in this technique.

For the purposes of this research, a second delay is defined. It is termed pad delay, and consists of the delay in the affected signal path that results from the gates that are not undergoing illumination. In a signal path, there are typically several gates, and each of the gates will have a propagation delay associated with it. The sum total of the propagation delay of the gates not being examined in a signal path is the pad delay.

TIMING MARGIN DEFINITION

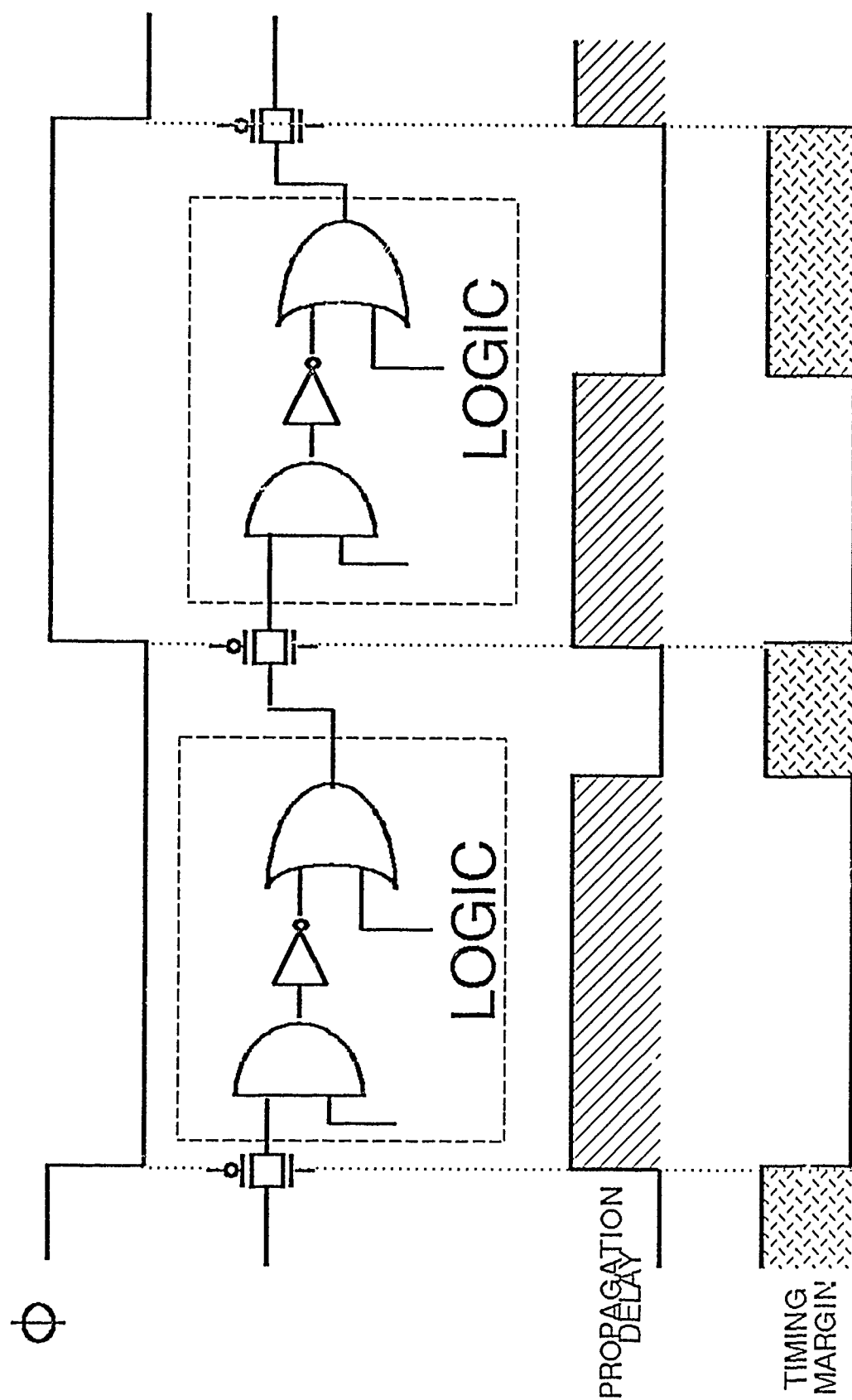


FIGURE 19

2.3.2 Timing Margin Measurement

As was mentioned earlier, the propagation delay variation of a gate induced by laser photocurrent injection is dependent upon many different variables. In a complex device, the threshold voltage, output load size, the transistor size, and other parameters vary slightly from gate to gate. Further, the efficiency with which the laser generates charge carriers is subject to the beam size and intensity, reflectivity at the semiconductor surface and at thin film boundaries, beam placement, and each individual gate geometry. For this reason it is difficult to generate a coefficient that relates a change in propagation delay to the intensity of an incident laser beam. An indirect method of measuring the propagation delay, which does not require this coefficient, must be used.

The method developed works independently of the transistor parameters and laser generation efficiency, so long as these parameters remain constant for the duration of the test. It relies on large signal MOSFET behavior curves.

There are two equations that describe the output voltage of a CMOS transistor pair. One is applicable in the saturation region of operation and one is applicable in the linear region of operation. For the purposes of this research, the effect of operation in the saturation region is negligible and may be discounted. The equation for the output voltage then becomes the voltage equation describing operation in the linear region, and may be written (from equation 23) as

$$V_{out} = (V_{dd} + .7) \exp \frac{2\beta(V_g - V_t)t}{C} \quad (28)$$

where V_t is the threshold voltage, β is the process transconductance, V_{dd} is the supply voltage, and C is the gate capacitance.

This equation contains some simplifying assumptions.

This equation describes an exponential curve, and is illustrated in figure 20. The propagation delay may be defined as the time between the moment that the input voltage crosses the $V_{cc}/2$ voltage level and the moment

the output voltage crosses the $V_{cc}/2$ voltage level. Neglecting the input transition time as small, the propagation delay may be measured directly off of the horizontal axis of figure 20.

Laser photocurrent injection will add an additional current that shifts the curve downwards to decrease the propagation delay or upwards to increase the delay. Decreased delays are not of interest in this application. As shown by figure 21, by shifting the curve one can find the new propagation delay by determining the new $V_{cc}/2$ crossover time. Note that this variation in crossover time does not vary linearly with laser intensity, but exponentially. Figure 22 shows the variation of propagation delay with laser intensity.

Figure 22 reveals two pertinent facts. First, there is an intensity beyond which the logical operation of the gate will be overridden such that the logic level is determined by the laser intensity and not the gate input voltages. Secondly, the laser effect changes with intensity in such a way that small changes in high laser intensities have a much greater effect than small changes in low laser intensity.

One may draw an analogy between the voltage-current diode curve and the intensity-propagation delay curve. Just as small changes in large voltages biasing a diode bring about large changes in current, small changes in high laser intensities bring about large changes in propagation delay. This phenomenon limits the use of this technique.

The curve of figure 22b shows the change in propagation delay of a CMOS gate. This is important in that the propagation delay of a signal path directly determines the maximum operating frequency for that path. This can be illustrated by the general case of a simple inverter placed between two latches. The first latch applies a signal to the input of the inverter, and the second latch stores the logical value of the output out the inverter output at the next active edge of the clock.

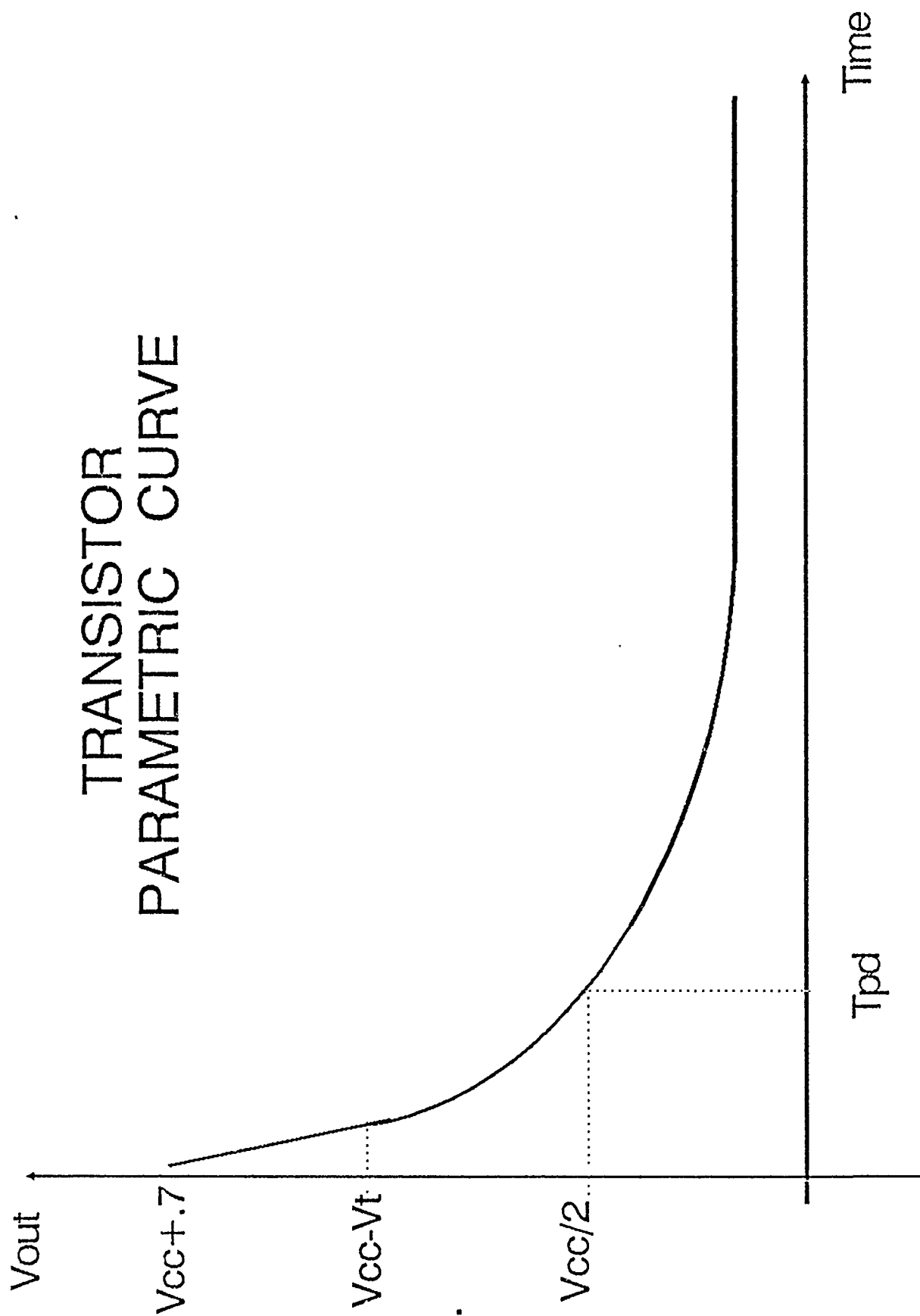


FIGURE 20

PHOTOCURRENT EFFECT ON TRANSISTOR PARAMETRIC CURVES

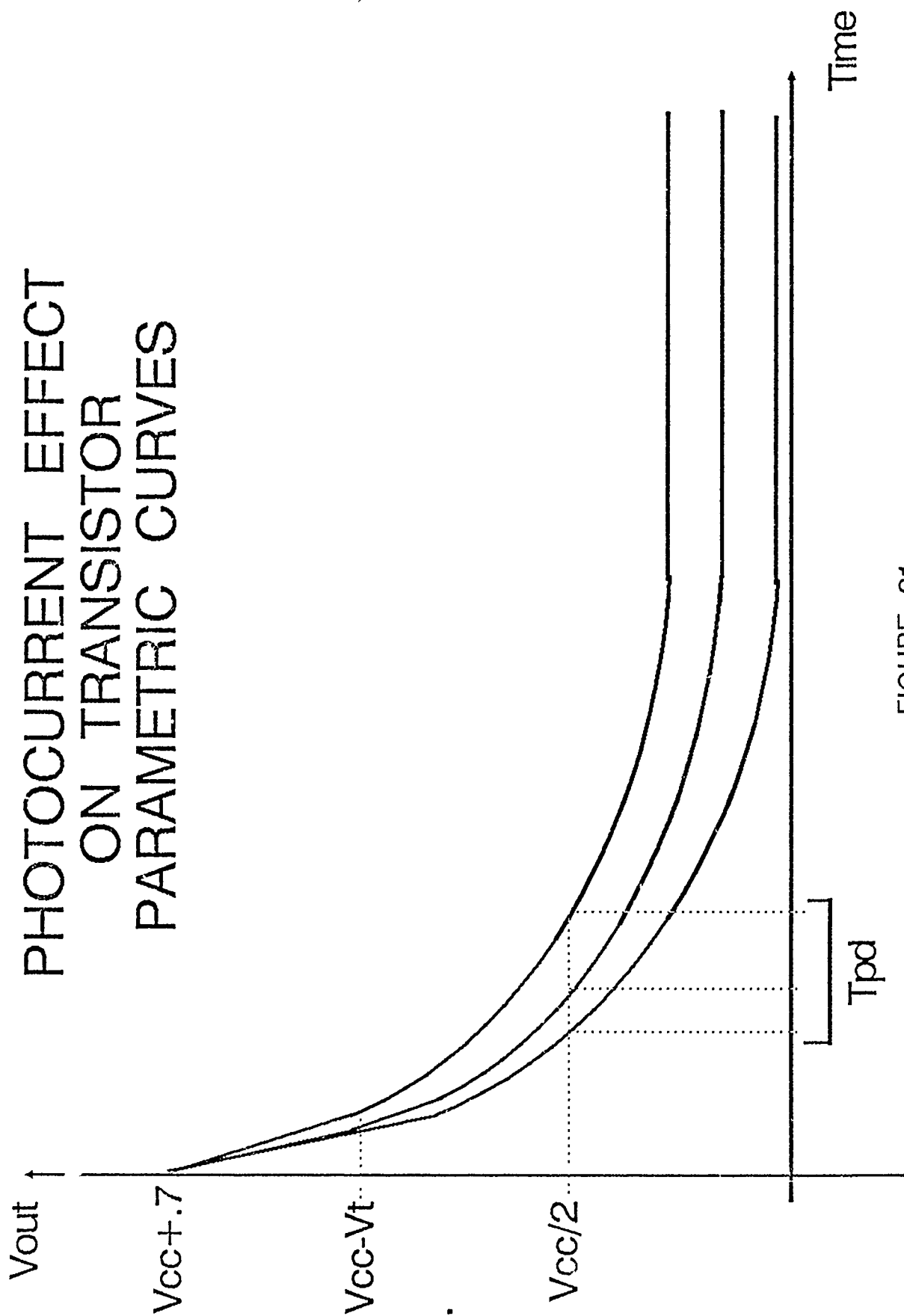


FIGURE 21

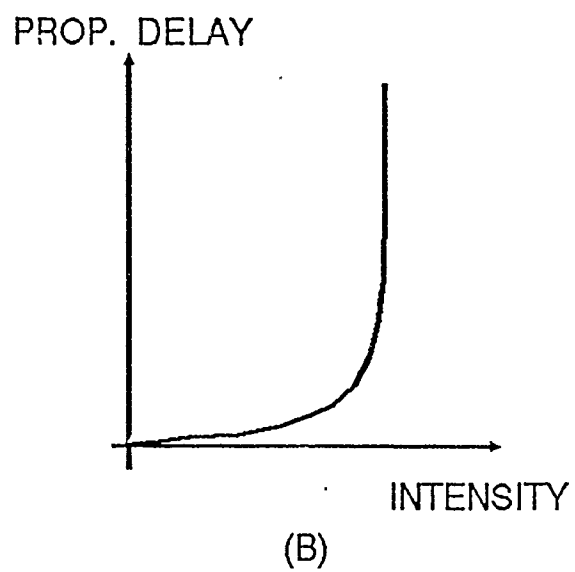
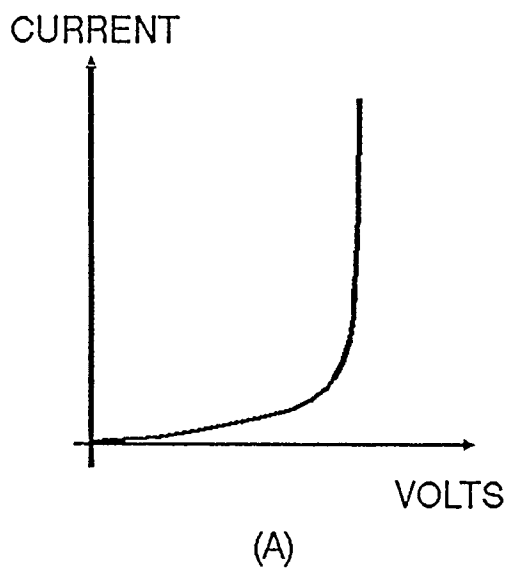


FIGURE 22

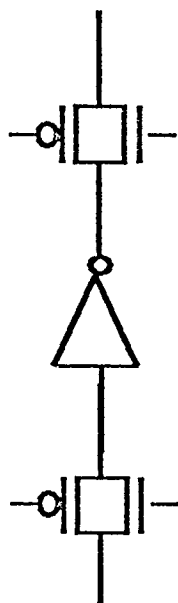
Laser illumination of the appropriate drain will increase the propagation delay. By making successive measurements of the maximum frequency at different levels of laser illumination, a curve of illumination verses frequency is generated. This curve is detailed in figure 6. In this figure, the maximum possible operating frequency occurs at F_{max} , and is determined by the unilluminated inverter propagation delay. Define the rail intensity is the intensity at which the laser determines the logical value of the inverter regardless of timing considerations.

The example of the inverter between two latches may be viewed as the most simple case of the general logical configuration of clocked circuits, that of logical gates forming a signal path with proper logical operation constrained by the timing of hardware latches. This general case view can also be applied to the signal paths of complex CMOS devices. Complex devices, however, have more than one signal path.

Complex devices have a maximum operating frequency for a given input vector that is a function of the timing margin of the most critical signal path in the device. By identifying this signal path and illuminating a gate in it in such a way as to increase the propagation delay through that path, the maximum operating frequency of the device would be reduced. Frequencies beyond the maximum allowable are identifiable by incorrect logic at the outputs of the device. The curve illustrating this illumination would look exactly like that of Figure 23.

If another signal path was identified and a gate in that path illuminated, there would not be a change in the maximum operating frequency of the test device until the illuminated path became the most critical path in the test device. Figure 24 illustrates the curve obtained by illuminating this node. It reveals no change in the maximum operating frequency until some intensity threshold is reached.

MODEL APPLICATION



NODE WITH MOST CRITICAL TIMING

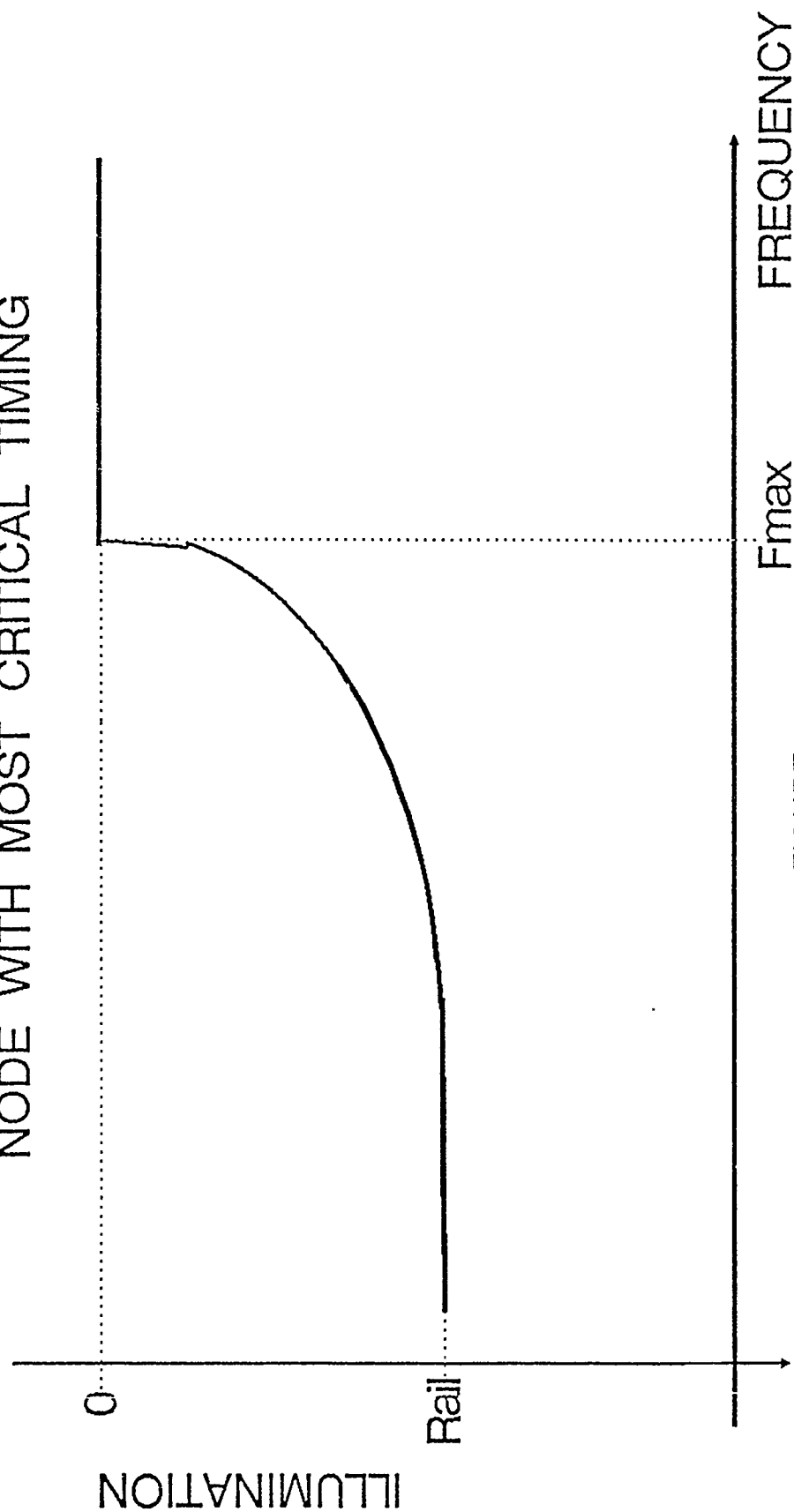
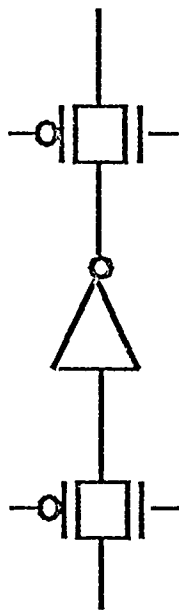


FIGURE 23

MODEL APPLICATION



NODE WITH CRITICAL TIMING

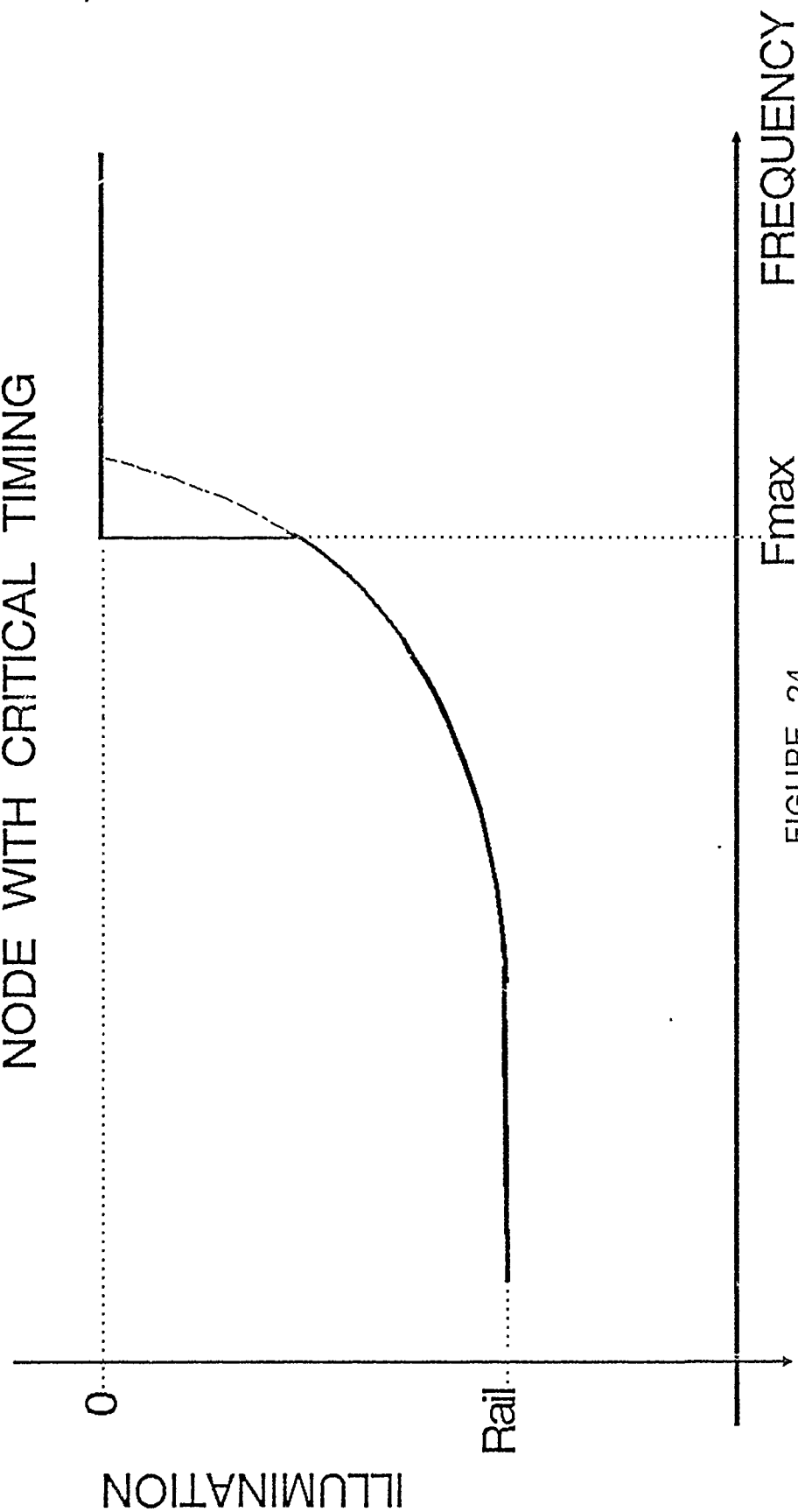


FIGURE 24

By projecting the curve of figure 24 back to the zero illumination axis, the timing margin of the illuminated signal path can be determined. This technique works independently of the transistor parameters or the laser intensity coupling parameters, so long as the laser has sufficient intensity to cause a timing failure in the illuminated signal path and form the curve of illumination verses frequency.

2.3.3 State Ranking

Once nodes with critical timing have been spotted, it is possible to determine the states of the DUT in which the illuminated node has critical timing for a given input vector.

There are three principles that make this possible. First, the semiconductor device parameters and laser illumination efficiency may be held constant for any given single node. This first assumption requires that the supply voltage be held constant, the laser position is held constant, and the laser maximum illumination intensity be held constant.

Second, propagation delay increases with increasing laser intensity. Third, propagation delays that are larger than the applicable clock frequency may be detected at the DUT outputs as logic errors.

To spot states with critical timing, each state must be illuminated individually by the laser. To do this, each clock cycle is illuminated by a laser pulse with only one clock cycle illuminated per test vector run. This requires a tight control on the laser pulse timing and width. States with a timing margin will be detected by logic faults at the DUT output. This is illustrated in Figure 25. Once these states are identified, they may be examined further.

The laser intensity necessary to just cause an output failure for each state can be determined. States with more critical timing will require less laser intensity to cause an output failure. Using these procedures, states with critical timing can not only be identified, but ranked in order of most to least critical timing.

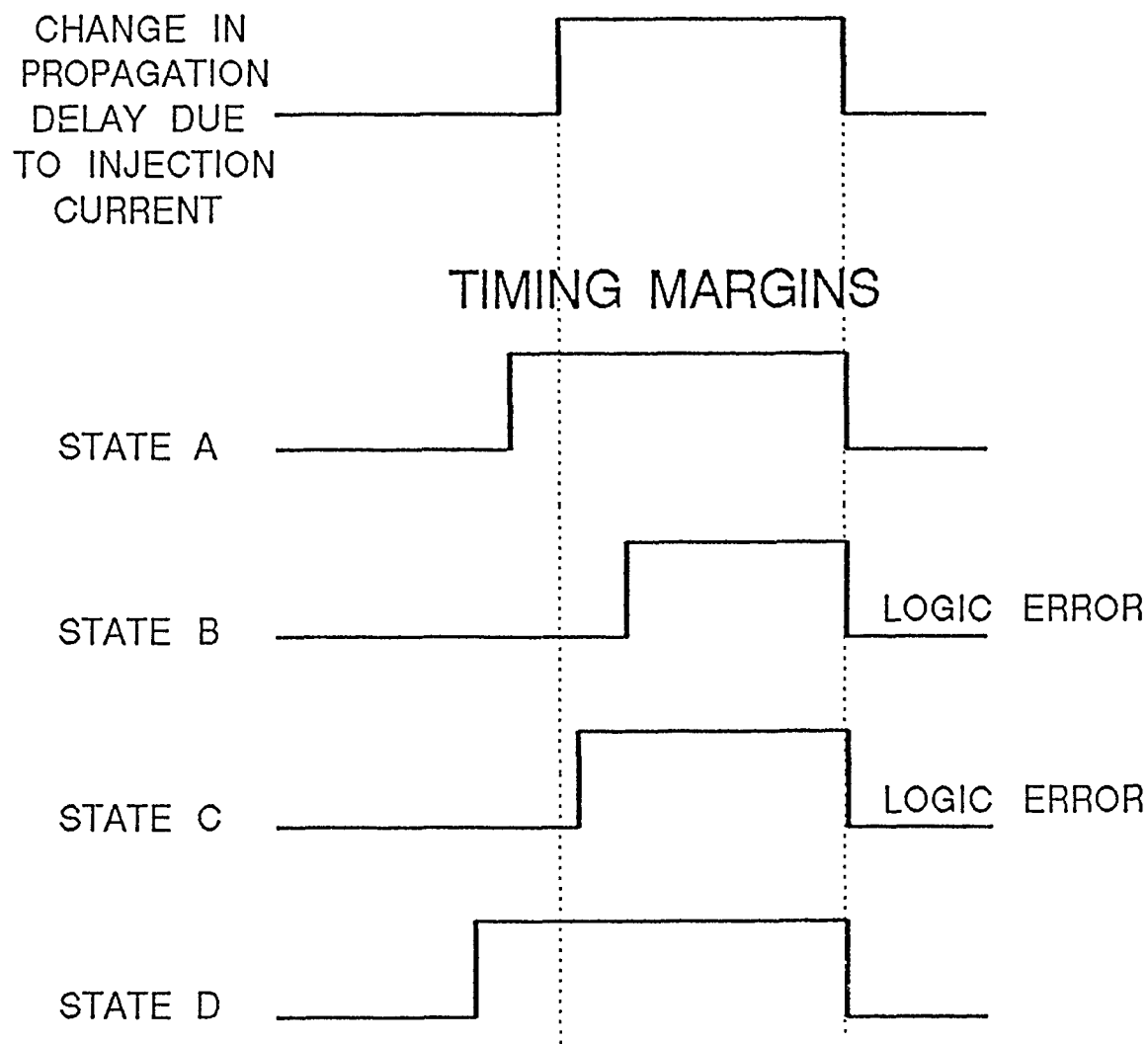


FIGURE 25

3 Simulations

3.1 Modeling of the Simple Device

The simulations to follow were conducted to prove the previous theoretical discussions of CMOS gate behavior, and to give the simulator some validity in proving itself against actual measured data.

3.1.1 Output Curve Simulation

The first simulation run was to produce output curves. With this, the curves are to be compared to those in the theory dealing with the "exact" model, and then with the greatly simplified model.

3.1.1.1 Device Model

The test setup is modelled as an inverter driving a load impedance and subjected to an injection current. The load impedance is the equivalent resistance and capacitance of the inverter output and of the input of the next inverter. The illumination injection current is the current source connected to the output of the inverter. This is shown in figure 26. The simulation results below apply for a rising edge only on the input and for the 2 volt and 5 volt supply scenarios. The input signal is modelled to have a 3ns rise time to match that of the actual input generator.

3.1.1.2 Parameter Extraction

This section explains all parameters but the photo injection current. Spice requires four major parameters for their MOSFET model (all of their minor parameters have defaults already consistent with CMOS design). The first is the process parameter transconductance (β), which was .00258 A/V² for the n-channel transistor, and .00261 A/V² for the p-channel transistor. The second is the threshold voltage (V_T), which was 0.6v for the n-channel transistor, and 0.85v for the p-channel. Both are estimated in chapter 2 under "Emperical Estimations of V_T and β ". The third parameter is transistor lambda

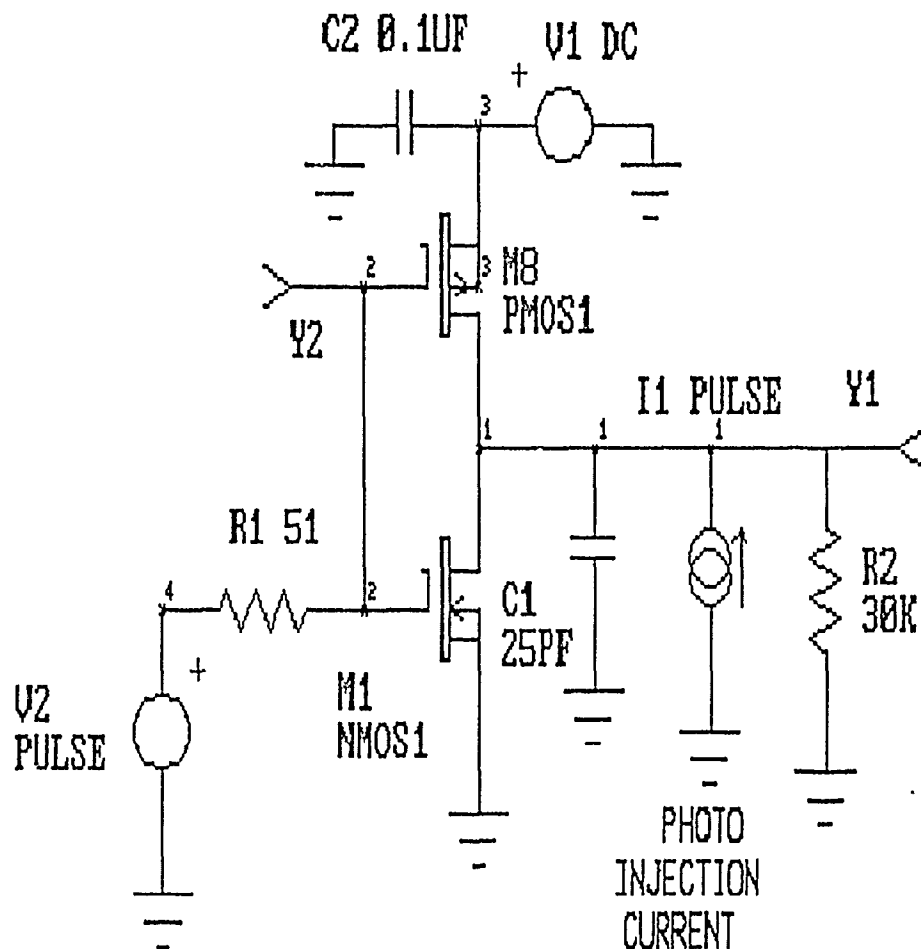


Figure 26: Model Schematic

(which is equivalent to bipolar transistor Early voltage.) A value of 0 was assumed for this, as the high current switching effects of the simulation would be hardly affected by this parameter. The fourth parameter is the surface potential. The SPICE default for this (0.6v) is accurate enough. The capacitance was not included in the above parameters, but was included in the model schematic. The capacitance of 25pF was obtained by summing the inverter output capacitance and all stray capacitance of the test setup (16pF.) This capacitance is represented as a simple capacitance between output and ground. The output resistance of the fixed timer was also included in the model (the 51 ohm resistor.)

3.1.1.3 Modelling Photoinjection

The photo injection current caused by the laser hitting a device was modelled as a current source. The current programmed into this source was acquired from the current data of the continuous illumination study. These currents are the currents plotted near the left and right edges of the continuous illumination plots. The polarity is determined by whether the n- or p-channel transistor is being illuminated. The current "sources" if the p-channel transistor is illuminated, and the current "sinks" if the n-channel transistor is being illuminated.

3.1.1.4 Simulation Results

Various Output Curves. The results of the simulation below in Figure 27 are for the 2 and 5 volt case, with n-channel, p-channel and no transistors illuminated. The results have the propagation delay located in the DIFF section of the graph header. The first set undergo no illumination. The second set undergo illumination to decrease the propagation delay. The third set undergo illumination to increase the propagation delay.

Comparison with Theoretical Models. Figure 28a is an illustration comparing the output curves of the simulation with the theoretical models. The two models are plotted explicitly with respect to each other, and the simulation is placed in this picture so as to best fit the "rigorous" theoretical model. This figure compares the simplified model to that of the rigorous model and simulation so as to give some reference to base the simplified model.

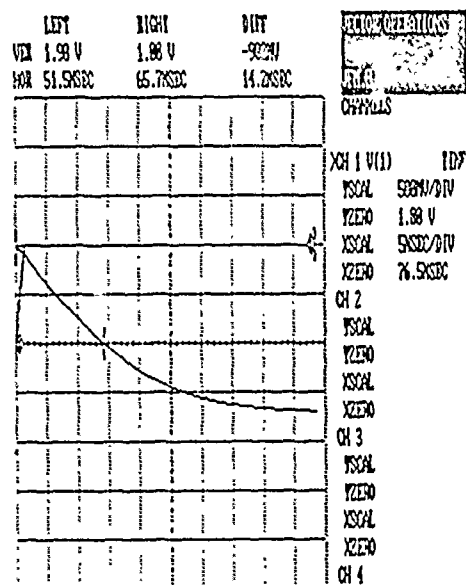


Figure 27a
Supply voltage of 2
volts
No injection current

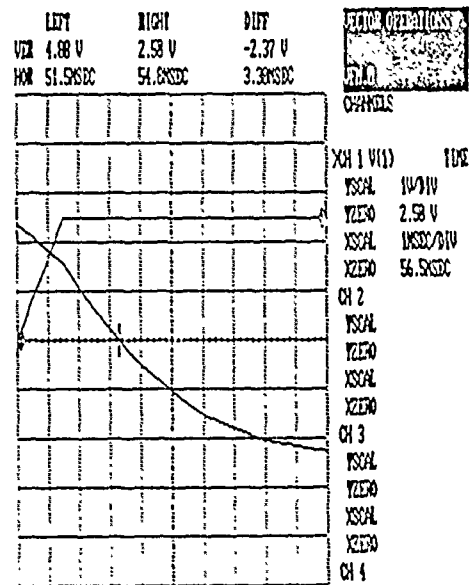


Figure 27b
Supply voltage of 5
volts
No injection current

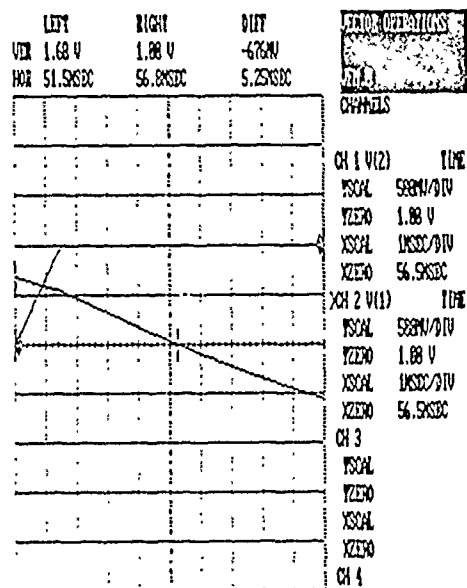


Figure 27c
Supply voltage of 2
volts
N-channel illuminated

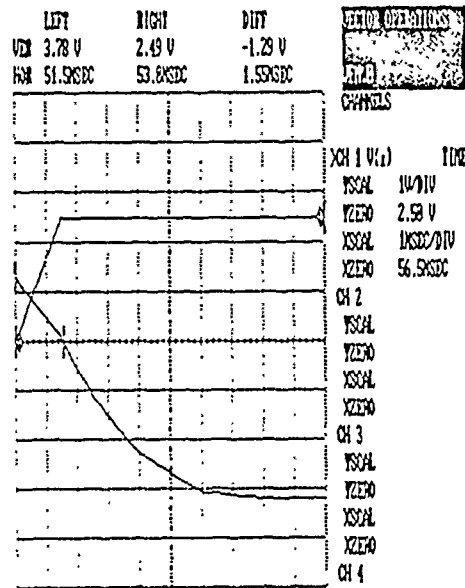


Figure 27d
Supply voltage of 5
volts
N-channel illuminated

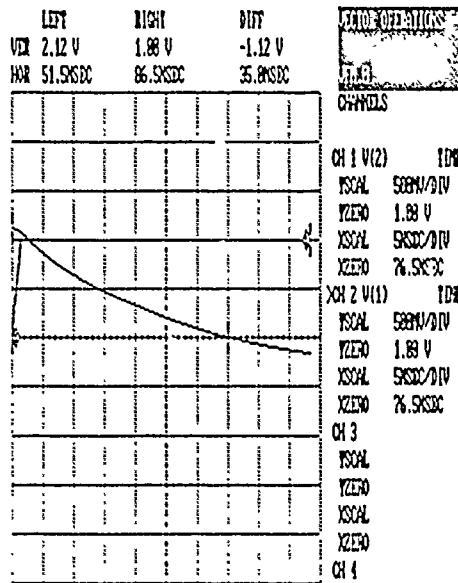


Figure 27e
Supply voltage of 2
volts
P-channel illuminated

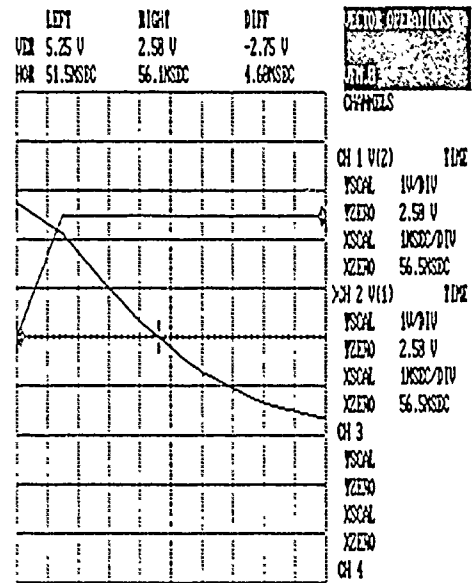


Figure 27f
Supply voltage of 5
volts
P-channel illuminated

Figure 28b compares the simulation on to the simplified model, which are compared. This figure shows the relative merit of using the simplified model in determining the propagation delay of the inverter.

3.1.2 Delay versus Illumination

This simulation has more use in the complex device test than here, but is entirely within the scope of the simple device test. The results of this simulation (Figure 29) clearly show that the propagation delay of the inverter changes with respect to illumination. The simulation was automated, with the source code provided in an appendix.

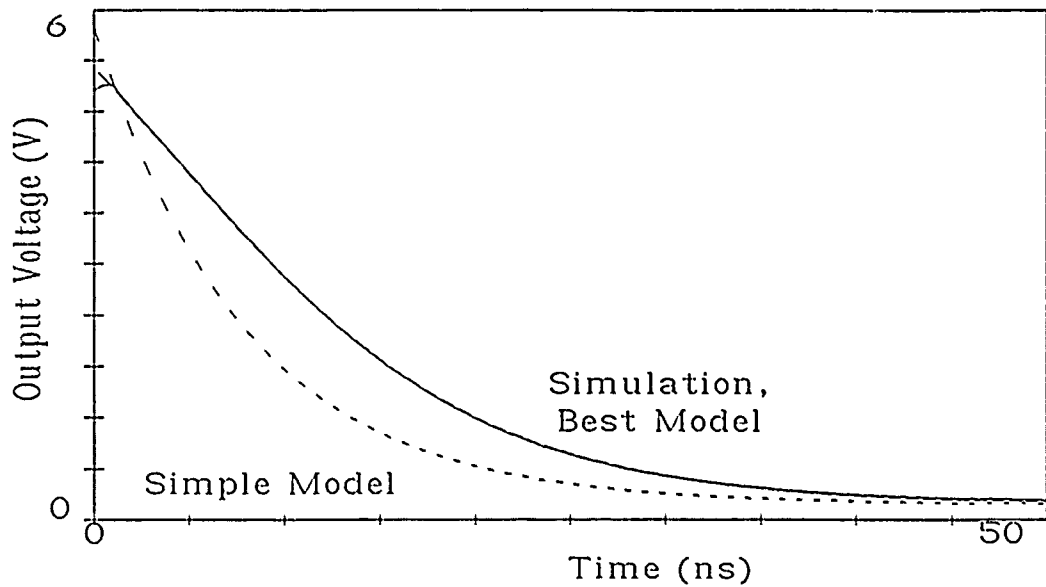


Figure 28a Output of inverter with respect to time. Spice simulation (solid line), "rigorous" model (dashed line), and simplified model (dotted line) compared. The rigorous model is hard to find; it is hidden under the simulation.

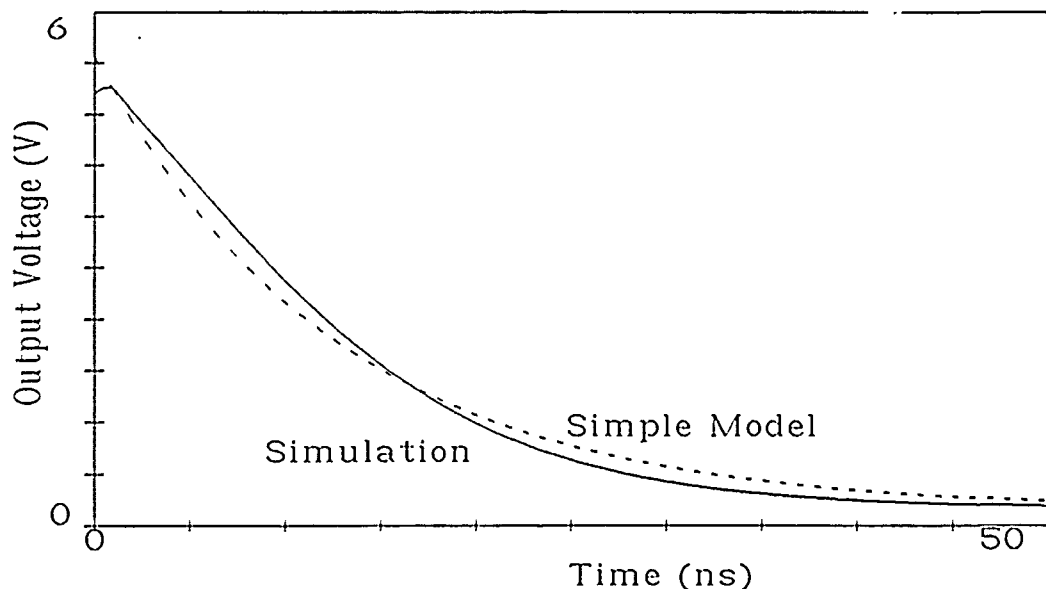


Figure 28b Output of inverter with respect to time. Spice simulation (solid line) with simple model (dotted line). Simple model designed to fit simulation, but requires an unknown and empirically determined alpha (beta) term.

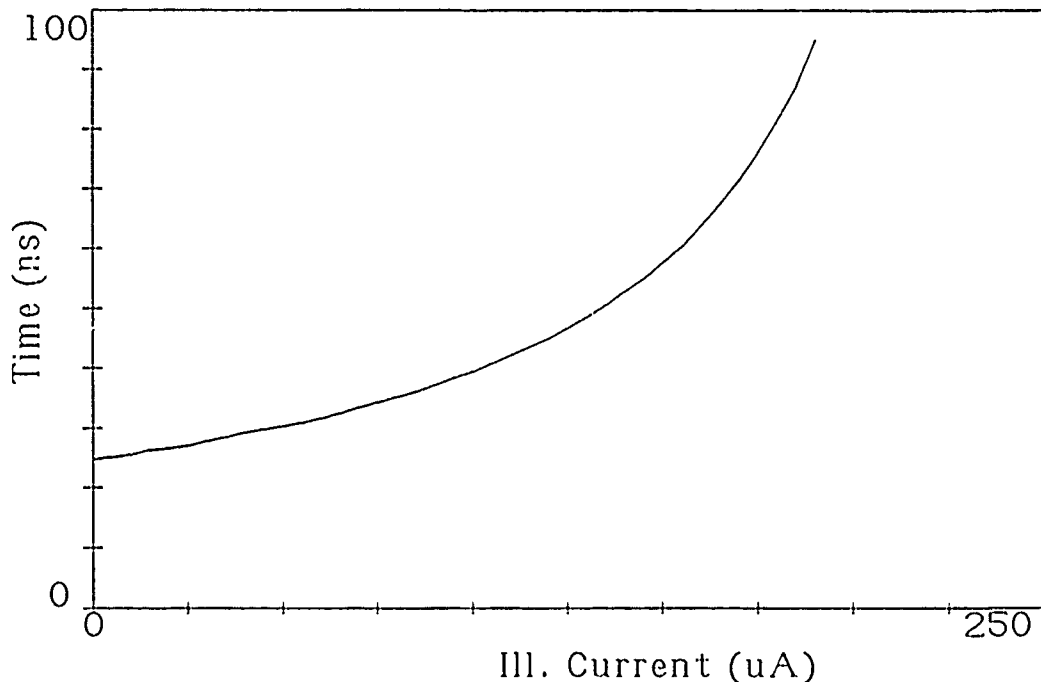


Figure 29. Effects of illuminating a transistor on the delay of an inverter. Figure is correlated Spice simulation data.

3.1.3 Pulse Simulation

The third part of this simulation deals with presenting curves that will fit with the measured data in the pulsed illumination test sequence. This simulation is to show that the pulse illumination test can be simulated. This simulation is also automated, and follows the general trend of the previous simulation (with source code in Appendix 1), except that the illumination level is constant, but pulse delay and width vary. An example of this simulation is shown above in Figure 30, and will be used as a comparison against measured data in the next chapter.

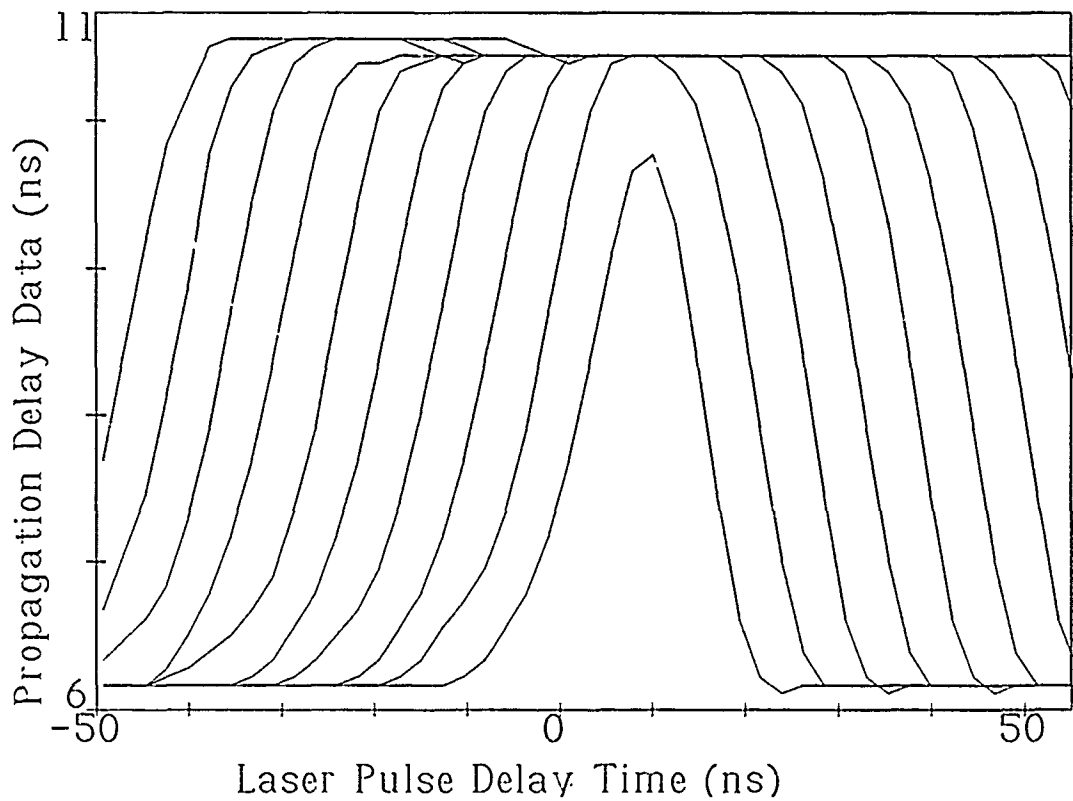


Figure 30 Spice simulation of pulsed illumination.

3.2 Modelling of the Complex Device

3.2.1 The Numerical Methods

3.2.1.1 Curve Fitting

The node raking experiment measures f , the maximum DUT operating frequency, and its associated L_{inj} , the laser intensity necessary to cause the DUT to fail at f . From the graphs of the experimental data two other values can be obtained. These are the lockout intensity L_0 and maximum frequency of operation f_{MAX} . The maximum operating frequency of the DUT under conditions of no illumination is f_{MAX} . The lockout intensity L_0 is the laser intensity necessary set the logic level of the gate regardless of input conditions. The lockout intensity may be read off of the far left hand side of the data curve, where the data approaches an asymptote. f_{MAX} may be found at the other end of the curve, where the truncated curve intercepts the zero illumination axis.

In an attempt to mathematically model the experiment, the entire test process was simulated using gate models of an inverter from SPICE and simulated random maximum frequency variations. This simple model of a signal path is not intended to represent all of the possible signal path architectures available in complex CMOS circuitry today, but is instead intended to provide one modeled representation of a signal path architecture. The test procedure simulation used the same data sampling scheme as the experimentation, and a frequency variation probability density function taken from the DUT under conditions of zero illumination. Frequency variations in the test data made Monte Carlo simulations necessary in order to test the numerical methods developed for determining timing margin.

The noise present in the data made it necessary to develop a numerical method which estimates the f versus L_{inj} curve from the experimental data. This best fit curve may then be projected back to the zero illumination axis in order to determine the relative timing margin at each node.

A review of what is expected from the data is useful at this time. The curve represents a series of frequencies f and the illumination intensity I_{inj} , necessary to cause a timing logic failure at those frequencies. It is expected that the data will take on an exponential shape, with an intercept on the illumination equals zero axis and a tail becoming asymptotic to some illumination level L_0 . L_0 is the illumination intensity necessary to set a logic level in the gate. The upper portion of the exponential curve will in general be truncated. This truncation is the result of some more critical signal path limiting the maximum frequency f_{MAX} of operation of the DUT.

Data taken above f_{MAX} is not useful to a curve fitting program. This data will be flat, and shows only that the DUT does not work above the maximum frequency of operation. Data below f_{MAX} is useful for curve fitting.

Equations will be derived which convert the experimental data to the form $y = Bx + A$ such that the variables x and y may be found using the experimental data. The variables B and A may be solved for using least square regression yielding

$$B = \frac{n\sum xy - \sum x \sum y}{n\sum x^2 - (\sum x)^2} \quad (29)$$

$$A = \frac{\sum y - B\sum x}{n}, \quad (30)$$

with a "goodness of fit" index of

$$G = \frac{n\sum xy - \sum x \sum y}{\sqrt{(n\sum x^2 - (\sum x)^2)(n\sum y^2 - (\sum y)^2)}}. \quad (31)$$

The variable G is the "goodness of fit" of the data.

3.2.1.2 Device Propagation Delay and Current Injection

In order to apply the regression technique, a linear equation must be developed that describes the expected curve of the data.

Let a CMOS inverter be regarded as the simplest form of a CMOS gate in one possible representation of a CMOS signal path. The schematic below illustrates the gate, with the p-channel transistor above and the n-channel transistor below. The input is tied to the gates of both inverters. When an input signal is applied to the gates, one of the inverters conducts, while the other inverter takes on a high impedance, with the capacitive output determining for the most part the rate at which the inverter changes state. Injected current which is opposite in direction to the current of the conducting transistor will increase the propagation delay. Only increased propagation delays will be considered in this derivation.

Consider the case of the n-channel transistor conducting. The charge stored in the output load will be conducted through the n-channel transistor to ground. The transistor will go through two different modes of operation, the saturation and the linear mode. Conduction begins in the saturation mode, with the drain voltage higher than the difference between the gate and threshold voltages. In this mode of operation, the stage has a linear voltage to time output relationship. This mode of operation exists for only a short period of time as the input voltage rises quickly to the V_{dd} voltage rail.

The linear mode of operation is characterized by a linear resistance generated by the transistor. This forms a resistive-capacitive circuit, and develops an exponential decay of the output load voltage. This mode of operation accounts for most of the propagation delay.

The saturation mode of operation may be viewed as an extension of the exponential curve which results from the linear mode of operation. This allows the saturation mode to be neglected. This assumption will not generate a large error as the saturation region does not exist for long. With this assumption, the equation of voltage and time for the case of the n-channel transistor conducting may be written as

$$C_l \frac{\partial V_o}{\partial t} = -\frac{V_o}{R_n} \quad (32)$$

with the solution

$$V_o = V_{cc} e^{\left(-\frac{t}{R_n C_l}\right)} \quad (33)$$

where V_o is the output voltage,

V_{cc} is the supply voltage,

t is time,

R_n is the n-channel transistor

equivalent output resistance,

and C_l is the load capacitance of the inverter.

The combination of R_n and C_l appear so often in these equations that another term, α (alpha) will be defined so that

$$\alpha = 1/(R_n C_l). \quad (34)$$

The exponential is then

$$V_o = V_{cc} e^{-\alpha t}. \quad (35)$$

For the case of the n-channel transistor conducting, the drain of the p-channel transistor will be illuminated in order to increase the propagation delay. The illumination creates an injection current I_{inj} , which must be added to the initial differential equation. This equation now becomes

$$C_l \frac{\partial V_o}{\partial t} = I_{inj} - \frac{V_o}{R_n} \quad (36)$$

with the solution

$$V_o = V_{cc} e^{-\alpha t} + (I_{inj} R_n)(1 - e^{-\alpha t}). \quad (37)$$

The above equation assumes that R_n is constant. I_{inj} is the injection current.

The propagation delay of an inverter may be defined as the difference in time between the instant the input crosses the $\frac{V_{cc}}{2}$ voltage level and the instant that the output crosses the $\frac{V_{cc}}{2}$ voltage level.

Let us assume that the output does not change at all until the input voltage crosses the $\frac{V_{cc}}{2}$ voltage level.

An equation for the propagation delay may then be calculated which is independent of the input conditions. This equation is

$$\frac{V_{cc}}{2} = V_{cc} e^{-\alpha \tau_{pd}} + (I_{inj} R_n)(1 - e^{-\alpha \tau_{pd}}), \quad (38)$$

or,

$$\tau_{pd} = \frac{1}{\alpha} \ln \left(\frac{V_{cc} - I_{inj} R_n}{V_{cc}/2 - I_{inj} R_n} \right). \quad (39)$$

In the above equations, τ_{pd} is the propagation delay of the inverter. The propagation delay is shown to depend on the supply voltage of the inverter and the injection current. The proper operating range for the τ_{pd} equation is the case where both the numerator and the denominator inside the logarithm are positive.

Two singularities exist in the τ_{pd} equation. The singularity in the denominator $V_{cc}/2 = I_{inj} R_n$ occurs when the injection current becomes the dominant current in the gate. When this occurs, the injection current sets the output logic level of the gate, and not the transistors. This situation may be called "device lockout," and its presence denies the gate operation regardless of input conditions. The injection current level I_o when this situation occurs is

$$I_o = \frac{V_{cc}}{2R_n}. \quad (40)$$

This is an important equation, and is used to calculate the timing margin in the regression technique. The other singularity (the one in the numerator) has no physical significance.

This derivation will yield similar results if carried out for the p-channel transistor conducting and the n-channel drain illuminated. The voltage

terms would be $V_{cc} - V$ terms, the n-channel current injection would generate a negative I_{inj} term, and the $V_o R_p$ in the differential equation would be positive.

3.2.1.3 Electrical Equations In The Regression Method

The experiments subject the DUT to illumination and determine whether or not a logic failure occurs at the DUT output. The curve formed by the experimental data forms the solution of a mathematical inequality, with logical errors occurring whenever the total delay T_{total} is larger than clock period $\frac{1}{f}$. The device will work whenever

$$T_{total} < \frac{1}{f}. \quad (41)$$

The term T_{total} consists of two different components. The first component is the propagation delay τ_{pd} of the gate as defined in the equations and text above. The second component is designated the pad delay T_{pad} and takes into account the other timing delays of the signal path. It accounts for the delay that arises from the other gates in the signal path that contains the gate under test. It further accounts for the delay that occurs when the gate inputs rise. This may be put into equation form for zero timing margin as

$$T_{pd} = \frac{1}{f} - \tau_{pad} = \frac{1}{\alpha} \ln \left(\frac{V_{cc} - I_{inj} R_n}{V_{cc}/2 - I_{inj} R_n} \right), \quad (42)$$

The equation may be written in an alternate form by dividing the top and bottom of the fraction within the logarithm by R_n . This yields

$$\frac{1}{f} - \tau_{pad} = \frac{1}{\alpha} \ln \left(\frac{V_{cc}/R_n - I_{inj}}{V_{cc}/2R_n - I_{inj}} \right). \quad (43)$$

Notice that two of the terms within the fraction closely match the equation for I_o in the derivation above. If I_o is known, then V_{cc} and R_n can be

eliminated from the above equation. When the formula for I_o is substituted into the equation above, we find that

$$\frac{1}{f} - \tau_{pad} = \frac{1}{\alpha} \ln \left(\frac{2I_o - I_{inj}}{I_o - I_{inj}} \right). \quad (44)$$

Notice that this equation is not dependent upon either V_{cc} or R_n . Also, this equation is independent of illumination losses in the device. Given the fact that injection currents are proportional to laser intensities, one may substitute a ϕL for the I terms above where ϕ is a constant of proportionality. This may be done because the currents induced in the DUT are proportional to the incident laser intensity. Performing this substitution, we find that ϕ cancels out on both sides.

Solving the above equation for intensity gives

$$L_{inj} = 2L_o \frac{\left(1/2 - e^{-\alpha \left(\frac{1}{f} - \tau_{pad} \right)} \right)}{\left(1 - e^{-\alpha \left(\frac{1}{f} - \tau_{pad} \right)} \right)}. \quad (45)$$

This is the operation boundary equation, and describes the maximum frequency of operation for the DUT for a given intensity level, and so describes the line tracing the border of proper operation of the DUT and DUT failure. This equation defines L_{inj} but only holds true below the unilluminated maximum frequency (f_{MAX}) of operation of the DUT.

The operation boundary equation and its related equations have five variables. Three of these variables (L_o , L_{inj} , and f) are known. The other two variables α and τ_{pad} are unknown. By multiplying the equation

$$\frac{1}{f} - \tau_{pad} = \frac{1}{\alpha} \ln \left(\frac{2L_o - L_{inj}}{L_o - L_{inj}} \right). \quad (46)$$

by alpha, this equation can be fit into the linear regression technique above, with

$$x = \frac{1}{f}, \quad (47)$$

$$y = \ln \left(\frac{2L_o - L_{inj}}{L_o - L_{inj}} \right), \quad (48)$$

$$A = -\alpha \tau_{pad}, \quad (49)$$

and

$$B = \alpha. \quad (50)$$

From this, α and τ_{pad} can be found. These values are used to represent the data in a clean format. With these values, the regression technique can be used to calculate the timing margin associated with each curve.

The timing margin equation, which is the general form of equation (41) may be written as

$$TM = \frac{1}{f} - T_{total}. \quad (51)$$

Here, the timing margin is shown to be the difference between the total delay of the gates in the signal path (T_{total}) and the period of the clock $\frac{1}{f}$.

With the regression results, the timing margin may be found, as the term $\frac{1}{f}$ is known and the term T_{total} can be determined. The term T_{total} is the sum of τ_{pad} and τ_{pd} . τ_{pad} is solved for in the regression technique. τ_{pd} was shown earlier to be

$$\tau_{pd} = \frac{1}{\alpha} \ln \left(\frac{2L_o - L_{inj}}{L_o - L_{inj}} \right). \quad (52)$$

As the timing margin is determined under conditions of zero illumination, the term L_{inj} is zero and the term L_o drops out. The equation for timing margin then becomes

$$TM = \frac{1}{f} - \tau_{pad} - \frac{1}{\alpha} \ln 2. \quad (53)$$

Experimental analysis has determined that the timing margin must be measured from f_{MAX} , the maximum operating frequency of the DUT under unilluminated conditions. This is necessary because f_{MAX} drifts in time. The timing margins, however, appear to be scaled by the same phenomenon that causes drift in the maximum frequency. Because of this, the timing margin may be measured if the clock period $\frac{1}{f_{MAX}}$ is used as $\frac{1}{f}$ in the above equation.

3.2.2 Timing Simulations

Simulations were necessary during the course of the research in order to test the numerical techniques developed to determine the criticality of the timing associated with each node. These simulations were used to improve the numerical techniques, and to develop new ones.

Two different simulation runs were developed and used. The first simulation developed assumed no noise in the system, and was used to test the regression technique on data gathered under simulated but ideal conditions. The second simulation series involved introducing noise into the system numerically. This Monte Carlo simulation technique was used to test the regression technique on simulated noisy data, and to develop new techniques for spotting critical nodes.

The simulations were designed to emulate the steps and procedures of the experiment as much as possible. The general simulation algorithm for the Monte Carlo analysis is given below. The simulation of noiseless data was carried out in a similar manner. The algorithm alterations necessary to generate the noiseless data simulations are described at the end of this section.

3.2.2.1 The Logic Analysis Kernel

The heart of the simulator is the logical analysis kernel. This kernel is an algorithm used to determine if for a given set of input conditions, a logic failure would be seen at the outputs of the test

device. The kernel is used repeatedly in the simulation software. The kernel requires as inputs two curves and five values.

The first curve is a probability density function (PDF) describing the maximum frequency variation noise present in the DUT. There is a considerable amount of noise in the experimental data. Investigations carried out over the course of the experimentation indicated that the noise consisted of constant fluctuations in the maximum operating frequency of the device under test. In order to characterize this noise, the DUT was excersized 3000 times with the test vector while conducting the maximum frequency determination routine described in section 5.5.5. This yielded a probability density function describing the frequency variation of the DUT without illumination.

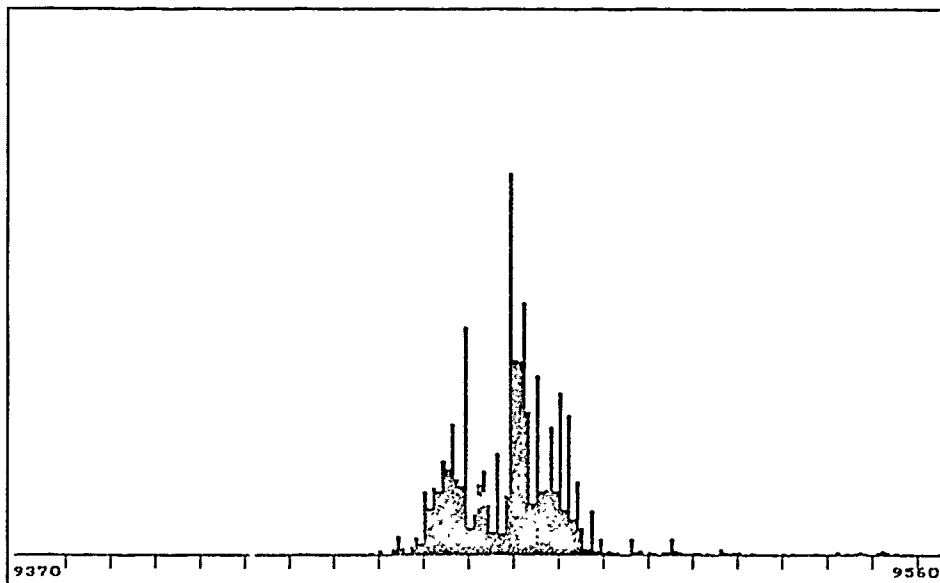


Figure 31: Probability Density of the Maximum Frequency Variation of the DUT. The x axis has units of kilohertz.

An algorithm exists to select a frequency so that the likelihood of its occurrence will reflect the likelihood of that frequency occurring in the PDF. To do this, each occurrence of a frequency in the PDF is assigned a unique integer value from 1 to 2996 (the total number of useful occurrences of a frequency in

the PDF). A random number from 1 to 2996 is then generated, and the frequency of the occurrence that corresponds to that random number is selected as the randomly selected frequency.

The second set of data necessary to carry out the simulation was a curve describing the propagation delay induced by a given level of laser illumination for a gate with a predetermined timing margin (TM). This curve was acquired through the SPICE simulation tools with laser photocurrent injection modeled as an additional current source between one transistor source and the output capacitive load.

To obtain the propagation delay verses laser intensity curve, transistor parameters and other model data were input into the SPICE program, as well as a simulated laser pulse intensity. The model output was a pair of curves, one of the input voltage versus time (the input voltage rises linearly to the voltage rail then stabilizes) and one of the output voltage verses time. These two curves were entered into an algorithm that determined the time at which each curve passed through the $V_{cc}/2$ voltage crossover level. The input crossover time was then subtracted from the output crossover time to yield the propagation delay associated with the corresponding simulated laser illumination level.

The simulation propagation delay test was run fifty times, each time varying the simulated laser intensity. The intensity and propagation data for the fifty tests was then entered into the P-I file. This new file was used by the kernel to determine the propagation delay associated with a given laser intensity for the simulated gate.

The kernel also required $f_{measure}$, the clock frequency of the DUT generated by the simulated frequency synthesizer, τ_{max} , the delay associated with the most critically timed signal path in the DUT, and TM, the timing margin selected for the node being simulated. The illumination level of the node under investigation must also be entered, as well as a correlation component, whose value is explained below.

The logic analysis kernel used the above inputs to determine the propagation delay associated with the

illuminated signal path, and to determine whether or not a logic error would be detected at the output of the DUT based on the internal delays and the given DUT clock frequency.

The propagation delay of the illuminated signal path was designated τ_{ill} , and was determined as follows. First, the mean maximum frequency of the frequency probability density function (MMF) was determined using a weighted average, such that

$$MMF = \frac{\Sigma(Freq \times N.O.)}{\Sigma N.O.} \quad (54)$$

where $Freq$ equals a frequency of test found in the probability density function, $N.O.$ equals the number of times a the maximum frequency occurred at the given frequency, and $\Sigma N.O.$ is the total number of occurrences at all frequencies. Next, the pad delay (τ_{pad}) is calculated using the mean maximum frequency, the timing margin, and the propagation delay of the inverter taken from the P-I file when $I=0$.

$$\tau_{pad} = \frac{1}{MMF} - TM - (PI \text{ at } I=0) \quad (55)$$

Next, a scale factor is calculated. The scale factor takes into account the possibility that the maximum frequency at the signal path with the most critical timing (under unilluminated conditions) may not be the same as the maximum frequency of the node under test. This could result due to localized temperature variations across the surface of the DUT. The measure of the correlation between the temperature effects on timing at the node under test and the temperature effects on timing at the signal path of most critical timing is the correlation component, α . α was intuitively chosen to be .9 during the simulation runs. The equation for the scaling factor (SF) is

$$SF = \frac{\alpha T_{max} + (1 - \alpha) T_{2max}}{T_{MMF}} \quad (56)$$

where T_{\max} is a time period, found by taking the inverse of a randomly chosen frequency from the probability density function, $T_{2\max}$ is some other time period found by taking the inverse of another randomly determined frequency from the PDF, and T_{MMF} is the inverse of the MMF of the probability density function. $T_{2\max}$ is selected in such a way as to be statistically independent of T_{\max} .

From the above equations, the propagation delay of the illuminated node τ_{ill} can be calculated using the equation below.

$$\tau_{ill} = SF(\tau_{pad} + PI \text{ at } I_{given}) \quad (57)$$

In the equation above, $PI \text{ at } I_{given}$ is the propagation delay associated with the laser illumination intensity entered into the kernel.

The kernel will next determine whether or not a logic error will be detected at the output of the DUT based upon the above equations. A logic failure will be indicated whenever $\tau_{\max} > \frac{1}{f_{measured}}$ or whenever $\tau_{ill} > \frac{1}{f_{measure}}$.

The output of the kernel is an indication as to whether or not a logic error will be detected at the outputs of the DUT.

In order to generate noiseless simulations, the terms T_{\max} and $T_{2\max}$ are set equal to $\frac{1}{MMF}$. This eliminates the effects of maximum frequency variation in the simulation.

3.2.2.2 The Test Procedure Simulator

The test procedure simulator emulates the node ranking portion of the experiment using the general case of the inverter between two latches as one possible representation of a signal path in a complex CMOS device. The simulation is intended to emulate the experimental test procedure as much as possible. To this end, much of code that makes up the test procedure simulator was taken directly from the experimental code. This section will describe the simulator's algorithm.

The first step is to determine the maximum frequency (MF) of the DUT. To do this five randomly determined frequencies are taken from the probability density function (PDF), and averaged.

Next, a Test_Window_Adjustment_Value is added to the MF of the DUT to determine the starting Frequency_Of_Test. During the experiments, the Test_Window_Adjustment_Value is a user selected value entered from the keyboard which selects the range of frequencies over which testing will occur.

Next, the frequency synthesizer is adjusted to set the DUT clock frequency to the Frequency_Of_Test, and the following routine is begun. Initiate a binary search through the logic analysis kernel with the laser illumination intensity as the object of the search with the intensity starting at half of the maximum power, and with the basis of the search being proper logical operation of the DUT. Correct logical outputs of the DUT will correspond to a positive result of the basis of the test. The search will yield the laser intensity necessary to just cause a logic failure in the DUT.

The above binary search method is next repeated 129 more times until a total of 130 tests for illumination level of failure have been made. With each new test, the Frequency_Of_Test is decremented by one kilohertz, so that 130 frequencies are tested. Note that during the Monte Carlo simulations, T_{\max} and $T_{2\max}$ are generated anew for each of the seven passes of each binary search routine.

The 130 points of illumination versus frequency are then stored in a file in the same manner that the experimental data is stored. The numerical methods developed for use on the experimental data may be applied to the simulated data. In this way, the numerical techniques may be tested on data with known timing margins. For purposes of nomenclature, one application of the test procedure simulator emulates one experimental test run, and may be called a simulation test run.

3.2.3 Additional Numerical Techniques

The numerical technique described above was applied to simulated data in order to test its effectiveness. The results revealed several weaknesses in the technique. Additional numerical processing was added to the code in order to improve the technique, and figures of merit were created in order to establish whether or not a node is likely to be critical as defined by the parameters of the test procedure. These figures of merit were developed based upon results taken from the test procedure simulator, and may not be valid for other CMOS signal path architectures.

The following section details the additional sequences that are applied to test data in order to better rank and identify them.

It was found that spurious noise occasionally appeared in the data. This noise consisted of inordinately large increases or decreases in the laser intensity necessary to cause a logic failure in the DUT. This noise has a direct effect on the outcome of the numerical method if it occurs in such a way as to change the value of L_0 greatly from its noiseless level. In order to reduce the effect of this noise on the simulation data, the laser intensities of the ten lowest tested frequencies are averaged, and L_0 is set equal to this average.

The timing margin determination technique is also heavily dependent upon finding the correct τ_{\max} . For this reason, a numerical technique was developed to determine τ_{\max} without the use of human judgement by detecting the start of the exponential curve in the data.

To detect the edge of this curve, the data is run through several processing steps. The original curve is passed through a difference detector, which calculates the difference between the laser intensity of the point under investigation and the laser intensity of the points adjacent to the one under investigation. The difference curve is then passed through a seven point median filter, and examined to determine τ_{\max} .

The median filter of the intermediate curve examines each intensity versus frequency point, and compares it

to the points around it. The median intensity value of the three points to the right and the three points to the left of the point in question is assigned to the intensity value of the point being examined. This filters out noise spikes. Any significant slopes that remain in the data after the mean filter are the result of chronic transition noise, but not single spike noise. This curve is labeled the difference curve, and is presented in the data as a curve of small plus signs at the bottom of the graphs.

This difference curve represents a crude form of numerical differentiation, with large changes in intensity from point to point corresponding to large slopes, and small changes in adjacent intensities corresponding to small slopes. The τ_{\max} frequency was heuristically determined to be when the value of the difference curve crosses the $L_0/20$ intensity level, where L_0 is the average of the ten left most intensities from the data curve. This technique has proven quite successful at determining the τ_{\max} frequency location on the curve of the actual data, as well as the Monte Carlo and noiseless simulation data.

When the regression technique was applied to simulated noiseless data, the technique proved to be accurate on simulated data whose timing margin was small. On data whose timing margin was large, the regression technique failed. The regression technique depends upon measuring the slope of the curve of the data. This was difficult, however, because very large timing margins become statistically indistinguishable from very small timing margins. This results from two phenomenon.

First, as described in Section 2, the effect of the laser is at its greatest near the tail of the curve when injected photocurrents are large, just as the effect of changes in voltage in a diode is at its greatest when the diode is operating under conditions of high current.

Second, the test involves determining the laser intensity that just causes a failure of the DUT, but this intensity is quantitized by the limits of a binary

search. The present experimental set-up quantitizes the laser intensity changes to approximately 1 percent of the maximum laser intensity exiting the Bragg Cell.

These two phenomena combine to make measurements of small changes in the slope of the curve illumination vs. frequency curves difficult. These small changes are all that separate the very small and very large timing margins from one another. As a result, the regression technique cannot differentiate the two. Additional techniques have been employed to numerically separate the larger timing margin nodes from the smaller timing margin nodes.

An additional ranking technique was developed after it was noticed that the data generated using the Monte Carlo simulator has a noise profile that varies between small timing margins and large timing margins. This difference is seen in the filtered curve "bump" of the difference curve in data with large timing margins. Large "bumps" correspond to an increased effect of noise on the data and occur in data with large timing margins. This increased width may be detected. Data with a width beyond a certain threshold is considered to be too noisy for nodes with small timing margins, and so is considered to indicate a node with a non-critical timing margin. A noise criticality indicator measures the width of the occurrence of the noise. Noise beyond a cutoff width is assumed to be caused by a non-critical node timing margin.

A second technique was developed after it was noticed that curves with critical timing have a gradual slope associated with the actual data in the lower frequency portion of the curve. Monte Carlo data with large timing margins will have a very flat slope, with noise developing in the region around τ_{max} . This noise may cause the regressive numerical method to suddenly "blow up" and indicate a very small timing margin, rather than the appropriately large timing margin.

To take advantage of this phenomenon, two techniques were developed. First, a noise detection scheme was created which starts on the left hand side of the difference curve and scans right, looking for changes in the value of the difference curve greater than $L_0/10$.

Once the frequency corresponding to this point is discovered, τ_{left} is defined. The point τ_{left} is located eight points to the left of the $L_o/10$ crossover point. If the noise in the data never reaches the L_o threshold level, the search stops at τ_{max} , and τ_{left} is defined as eight points to the left of τ_{max} .

Next, the slope of the curve left of τ_{left} is measured. The intensity at τ_{left} is examined, and if it has changed less than 12 percent from L_o , then the slope is assumed to indicate a node with a flat slope, and the node is assigned to have a non-critical timing margin. A slope criticality indicator is then defined a value of 1 whenever the slope indicates a critical node, and a slope of 0 whenever the slope indicates a non-critical node. The slope criticality indicator is the primary indicator of criticality.

Additionally, as the data to the left of τ_{left} is considered smooth, all of the data to the left of τ_{left} is used by the regression technique to smooth and project the curve. Data to the right of τ_{left} is considered noisy, and so is not used by the regression technique.

Both the noise magnitude technique and the slope magnitude technique for determining criticality are applied to each node tested. If the node tested is identified as being non-critical for either test, then it is assumed to be non-critical. If the node tested is found to be critical for both tests, the node is assumed to have critical timing.

The number of points between τ_{left} and the $L_o/10$ crossover level, the $L_o/10$ crossover level itself, the number of neighboring points used in the mean filter, and the threshold for the determination of τ_{max} were all determined heuristically. The presently selected threshold levels indicate that nodes generated using the Monte Carlo simulator with timing margins between 0 and 4.3 ns are designated to be critical nodes, nodes with timing margins between 4.4 and 8.9 ns may be designated either critical or non-critical, and nodes with timing margins larger than 9 ns are designated as non-critical nodes.

3.2.4 Simulation Data

3.2.4.1 Noiseless Simulation Data.

The data presented in this section was generated using the noiseless simulation kernel option in the simulator described above. The curve depicted by the line made up of x's is the simulated data under noiseless conditions. The curve depicted by the line of circles is the "smoothed curve" generated by the regression technique. The line on the bottom of each graph made up of plus signs is the difference curve described in the previous section. The timing margin determined by the regression method is displayed beneath the curves, while the actual SPICE generated timing margin of the curve is given in the figure title.

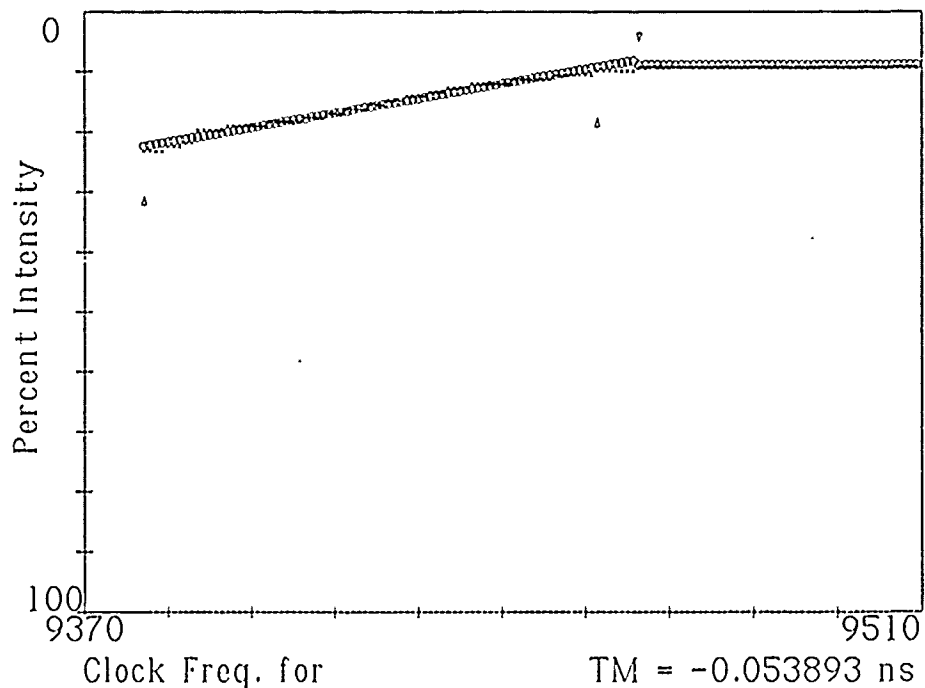


Figure 32. Noiseless Simulated Data with a SPICE Timing Margin of 0.0 ns.

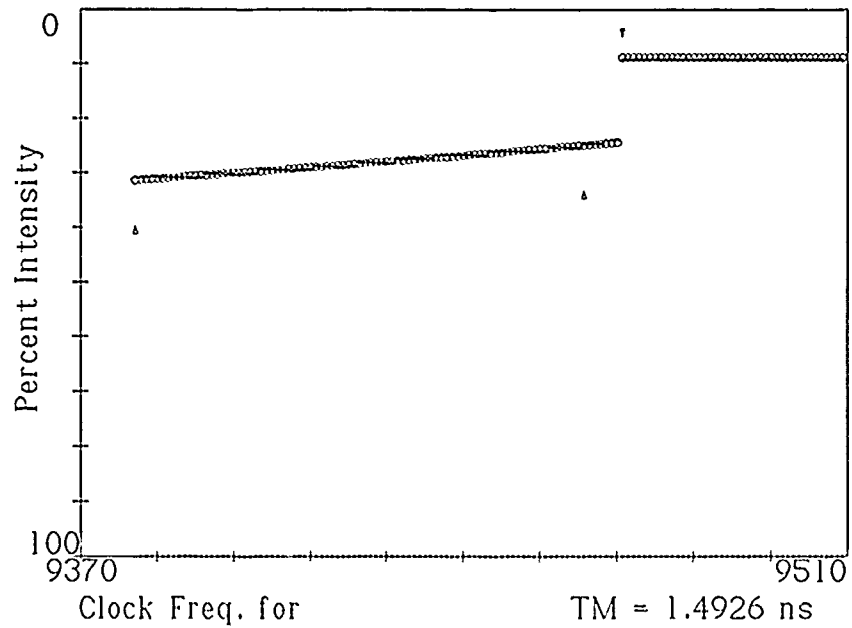


Figure 33. Noiseless Simulated Data with a SPICE Timing Margin of 1.0 ns.

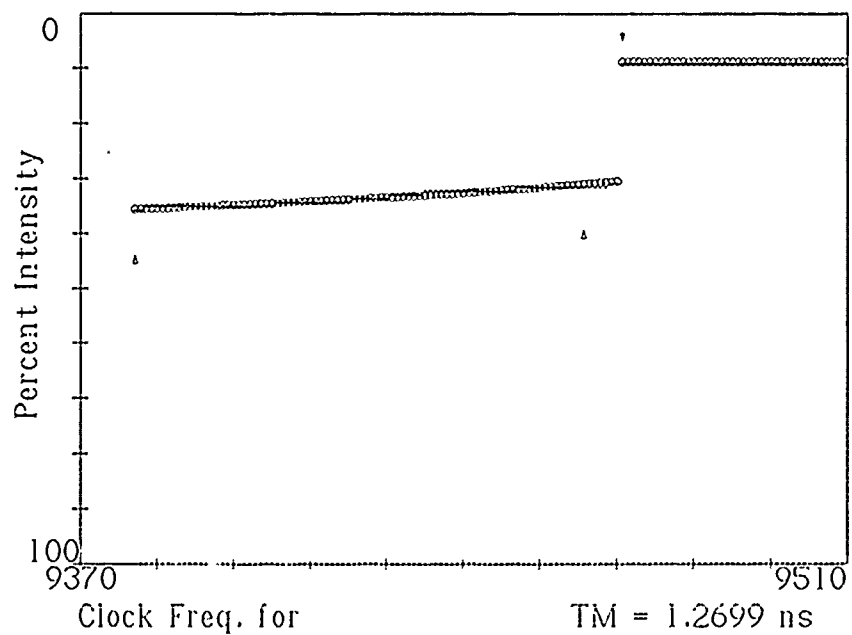


Figure 34. Noiseless Simulated Data with a SPICE Timing Margin of 2.0 ns.

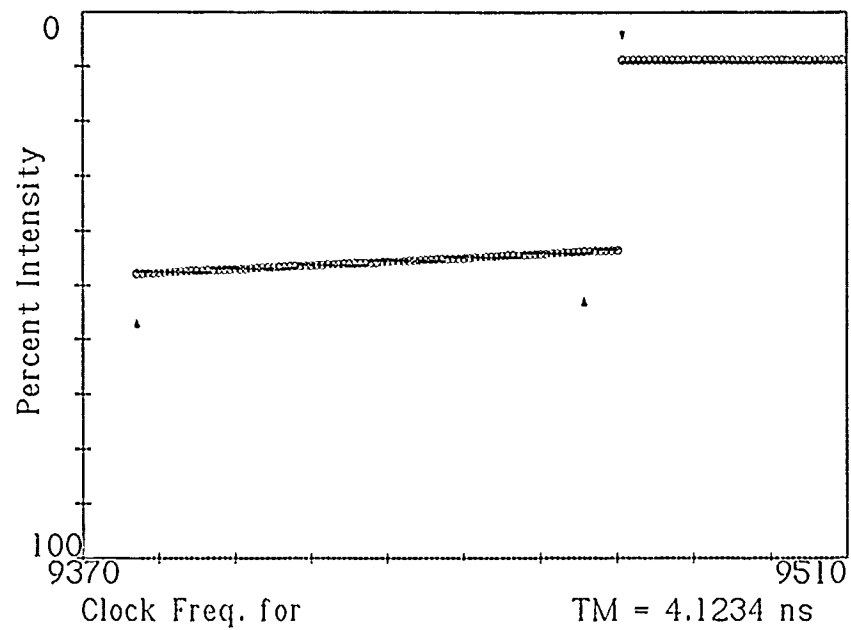


Figure 35. Noiseless Simulated Data with a SPICE Timing Margin of 4.0 ns.

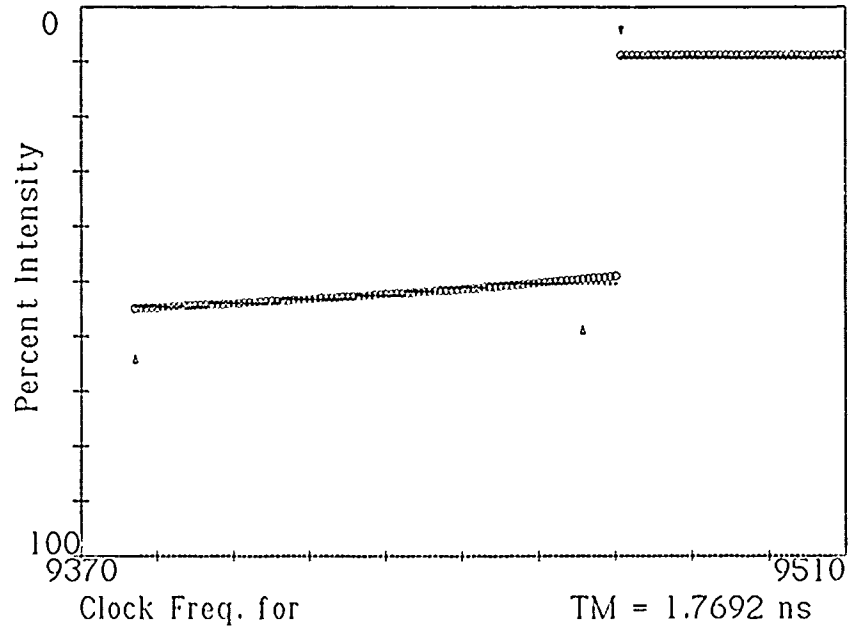


Figure 36. Noiseless Simulated Data with a SPICE Timing Margin of 6.0 ns.

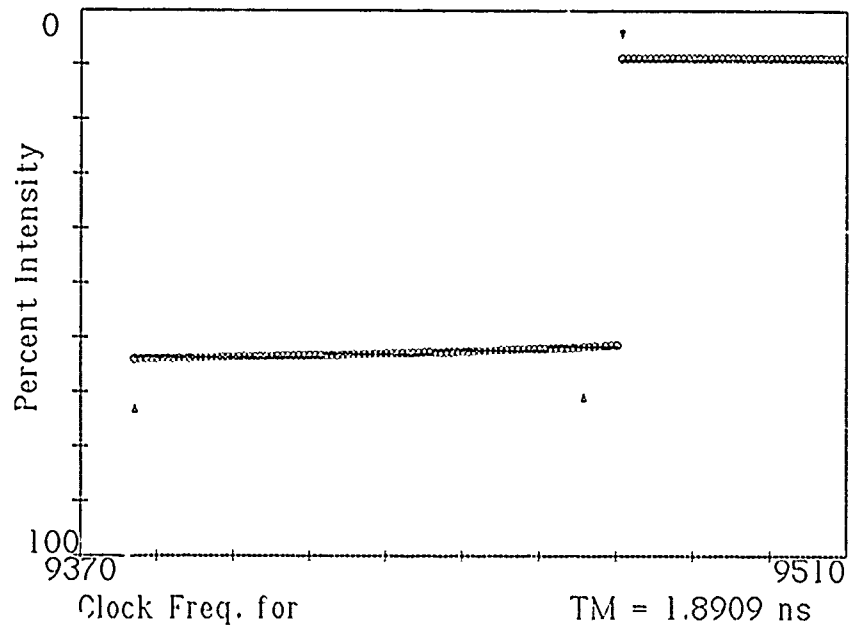


Figure 37. Noiseless Simulated Data with a SPICE Timing Margin of 10.0 ns.

As you can see, the regression technique is accurate on simulated data whose timing margin is small. On data whose timing margin is large, the regression technique fails. This failure occurs because the result of the regression formulas are highly dependent upon the shape of the data curve across the curve's entire length, while the value of the curve is quantized so as to appear flat as a result of the quantitized binary search data.

3.2.4.2 Monte Carlo Simulation Data

The data presented below presents the results of the Monte Carlo simulation of the experimental results. The data is presented in two different formats. The first format is the same as the one used to present the noiseless simulation data, with each simulation run generating three curves and a regression determined timing margin which is displayed in the illustration, and the actual SPICE generated

timing margin presented in the figure description. This format is used for Figure 38 through Figure 43.

The second format presents statistical data generated by conducting the Monte Carlo simulation five times on the same SPICE generated node. This format is used in Table 1 through Table 6. The numerical methods were applied to the results of each simulated data run, with the results given as a set of criticality indicators and statistics. The first five lines of data contain the criticality indicators for each of the five tests conducted on the node, with the first line containing the indicators for the first simulation run, the second line containing the indicators for the second run, and so on. The criticality indicators are described in the section titled Additional Numerical Techniques. CN is the noise criticality indicator. It indicates whether or not a node has critical timing by measuring the extent of the noise in the data. CC is the curvature criticality indicator, which indicates whether or not a node has critical timing by measuring the curvature of the data. In every case, a 1 corresponds to an indication that the node is critical, and a 0 corresponds to an indication that the node is not critical.

The sixth line data contains the overall criticality indicator. This indicator is consulted to determine whether or not the tested node has critical timing or not. The indicator occurs as a positive value only if both criticality indicators of a majority of the tests have a value of 1.

The seventh and eighth lines contain data generated by the regression technique. The term M displays the median of the five timing margins. The term A5 displays the average of the five timing margins, and the term S5 displays the standard deviation of the five timing margins. The fourth term, A3, shows the average of the three median timing margins and the term S3 displays the standard deviation of the three median timing margins of the simulated data.

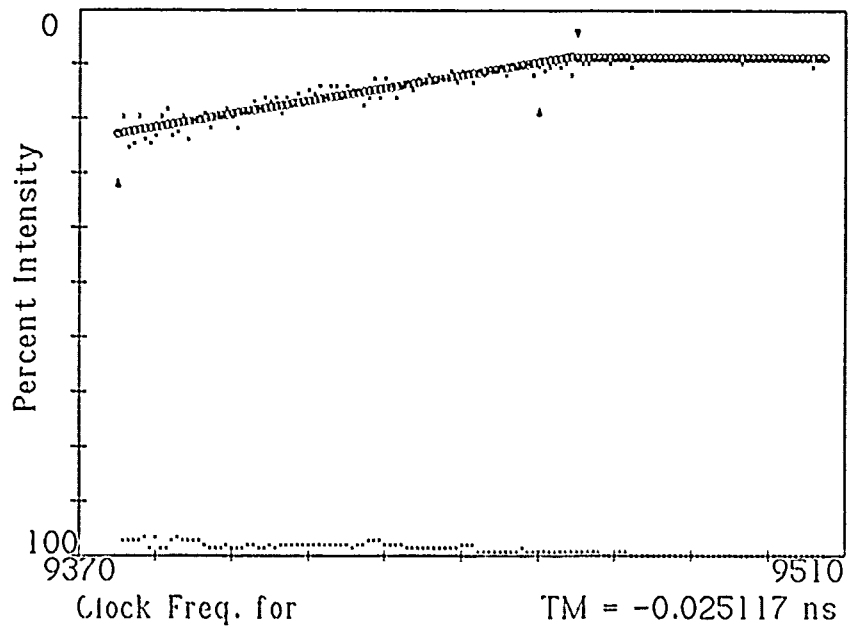


Figure 38. Monte Carlo Simulated Data with a SPICE Timing Margin of 0.0 ns.

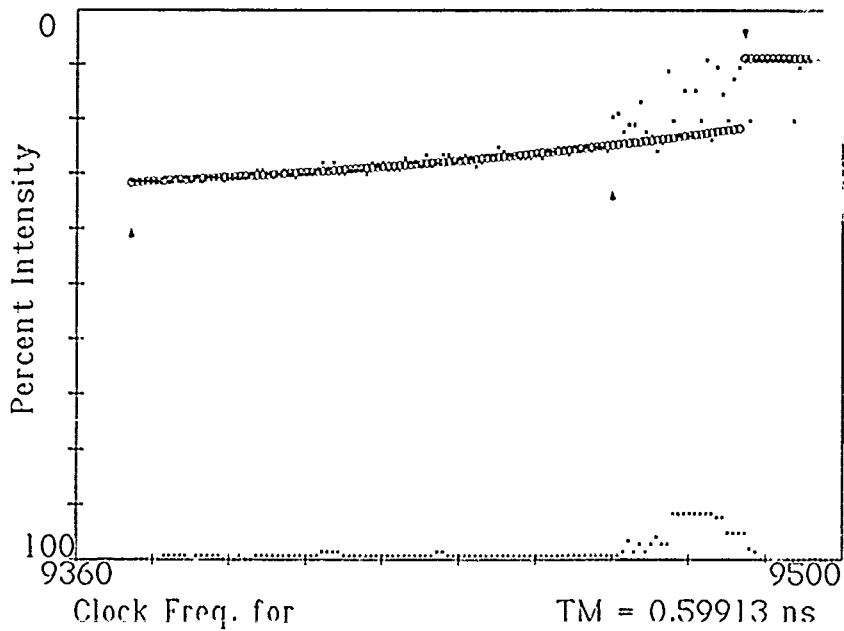


Figure 39. Monte Carlo Simulated Data with a SPICE Timing Margin of 1.0 ns.

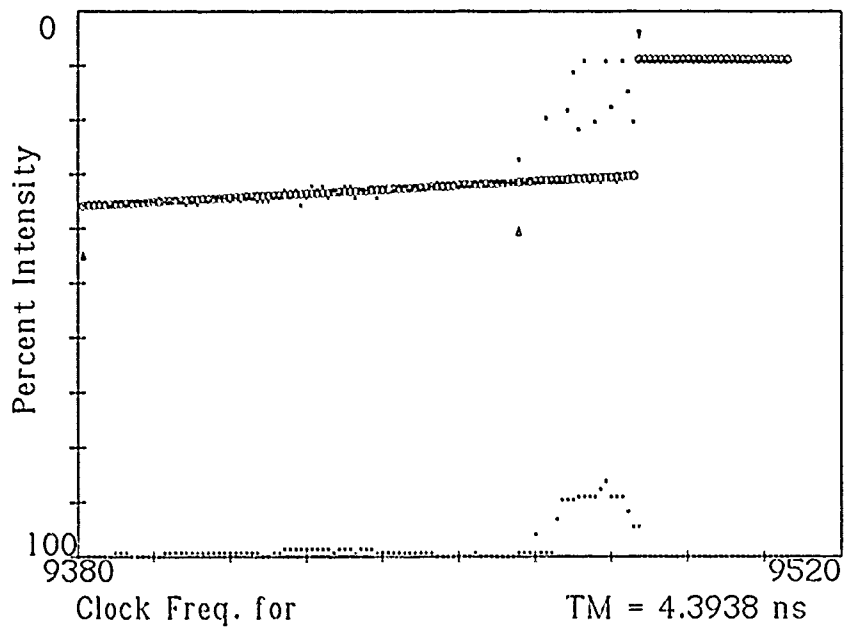


Figure 40. Monte Carlo Simulated Data with a SPICE Timing Margin of 2.0 ns.

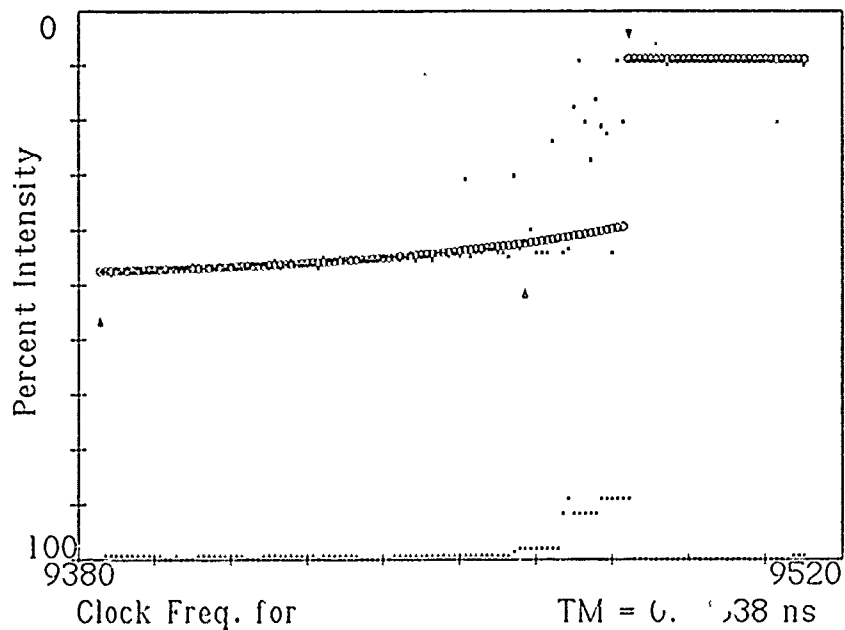


Figure 41. Monte Carlo Simulated Data with a SPICE Timing Margin of 4.0 ns.

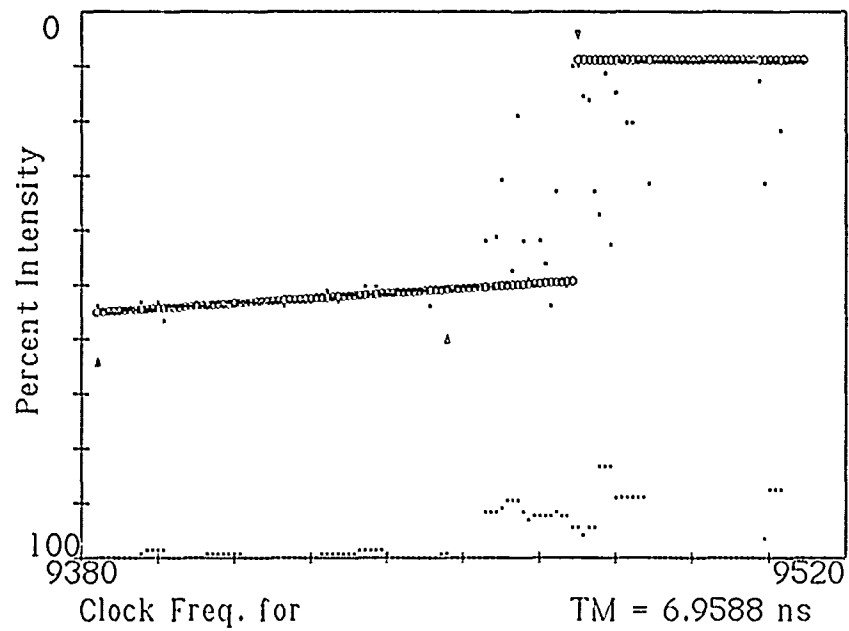


Figure 42. Monte Carlo Simulated Data with a SPICE Timing Margin of 6.0 ns.

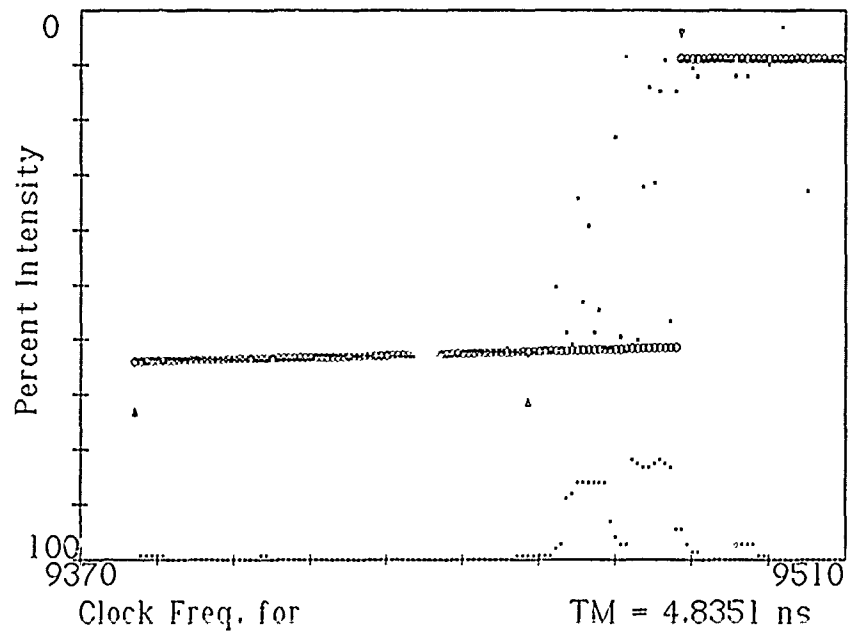


Figure 43. Monte Carlo Simulated Data with a SPICE Timing Margin of 10.0 ns.

TABLE 1

NODE STATISTICS AND CRITICALITY INDICATORS DATA OF A
 NODE WITH A SPICE TIMING MARGIN OF 0.0 NS USING A
 MONTE CARLO SIMULATION.

CN 0 = 1, CN 1 = 1, CN 2 = 1, CN 3 = 1, CN 4 = 1,	CC 0 = 1 CC 1 = 1 CC 2 = 1 CC 3 = 1 CC 4 = 1	
C=1		
M=0.0260650 9	A5=0.021120 88	S5=0.001180 636
A3=0.02934426,		S3=0.000210615

TABLE 2

NODE STATISTICS AND CRITICALITY INDICATORS DATA OF A
 NODE WITH A SPICE TIMING MARGIN OF 1.0 NS USING A
 MONTE CARLO SIMULATION.

CN 0 = 1	CC 0 = 1	
CN 1 = 1	CC 1 = 1	
CN 2 = 1	CC 2 = 1	
CN 3 = 1	CC 3 = 1	
CN 4 = 1	CC 4 = 1	
C=1		
M=1.043331	A5=0.946298	S5=0.109830
	2	6
A3=0.964266	S3=0.0333556	

TABLE 3

NODE STATISTICS AND CRITICALITY INDICATORS DATA OF A
NODE WITH A SPICE TIMING MARGIN OF 2.0 NS USING A
MONTE CARLO SIMULATION.

CN 0 = 1	CC 0 = 1
CN 1 = 1	CC 1 = 1
CN 2 = 1	CC 2 = 1
CN 3 = 1	CC 3 = 1
CN 4 = 1	CC 4 = 1
C=1	
M=0.606717	A5=1.359105 S5=2.131843
A3=0.6953856	S3=0.03291804

TABLE 4

NODE STATISTICS AND CRITICALITY INDICATORS DATA OF A
NODE WITH A SPICE TIMING MARGIN OF 4.0 NS USING A
MONTE CARLO SIMULATION.

CN 0 = 1	CC 0 = 1
CN 1 = 1	CC 1 = 1
CN 2 = 1	CC 2 = 1
CN 3 = 1	CC 3 = 0
CN 4 = 1	CC 4 = 1
C=1	
M=1.910455	A5=2.781174 S5=5.197485
A3=1.864467	S3=0.07735114

TABLE 5
 NODE STATISTICS AND CRITICALITY INDICATORS DATA OF A
 NODE WITH A SPICE TIMING MARGIN OF 6.0 NS USING A
 MONTE CARLO SIMULATION.

CN 0 = 1	CC 0 = 1	
CN 1 = 1	CC 1 = 1	
CN 2 = 1	CC 2 = 1	
CN 3 = 1	CC 3 = 1	
CN 4 = 1	CC 4 = 1	
C=1		
M=1.553508	A5=1.621746	S5=0.283645
A3=1.652458		S3=0.06943886

TABLE 6
 NODE STATISTICS AND CRITICALITY INDICATORS DATA OF A
 NODE WITH A SPICE TIMING MARGIN OF 10.0 NS USING A
 MONTE CARLO SIMULATION.

CN 0 = 1	CC 0 = 0	
CN 1 = 1	CC 1 = 0	
CN 2 = 1	CC 2 = 0	
CN 3 = 1	CC 3 = 0	
CN 4 = 1	CC 4 = 0	
C=0		
M=0.3481521	A5=1.804082	S5=3.563627
A3=1.433189		S3=2.59579

As can be seen from the Monte Carlo data, the timing margins of the nodes cannot be accurately determined or ranked using the regression technique. The standard deviation of the timing margins of nodes is statistically too great for the regression technique to be used to spot nodes with critical timing. It may, however, be used to examine nodes that are known to have critical timing. The noise and

slope magnitude criticality terms do, however identify which nodes have critical timing and which do not. With the present setting of criticality indicators, nodes which have a timing margin of approximately 4.3 ns or less will be identified as critical nodes, nodes with timing margins from approximately 4.3 ns to approximately 9.0 ns may be identified as critical nodes, and nodes with timing margins greater than approximately 9.0 ns will not be identified as critical nodes.

4 Simple Device Test

This chapter deals with collecting data from test runs in order to gather information about transistor characteristics, and to compare with the simulation results. Two items are NOT included in this chapter, but are presented later. The first is the collection of capacitance data by using an HP 4192A Impedance Analyzer as an attempt to properly model the inverter capacitance; the other is a test procedure and the corresponding results for testing timing effects on varying load capacitance. Both of these items are included in an appendix with explanations.

In this chapter, the necessary optics and circuitry for the simple device test are discussed. After that, the simple device test procedures are brought forth. The results of the simple device experiments are then compared to simulations of this test plan in the conclusion to this chapter.

4.1 Experimental Setup

4.1.1 Optical Components

The optical components consist of a HeNe laser, a Bragg cell with focussing optics and driver, and a microscope, as well as an optical table and several stages and positioning devices. A complete list of the components is as follows.

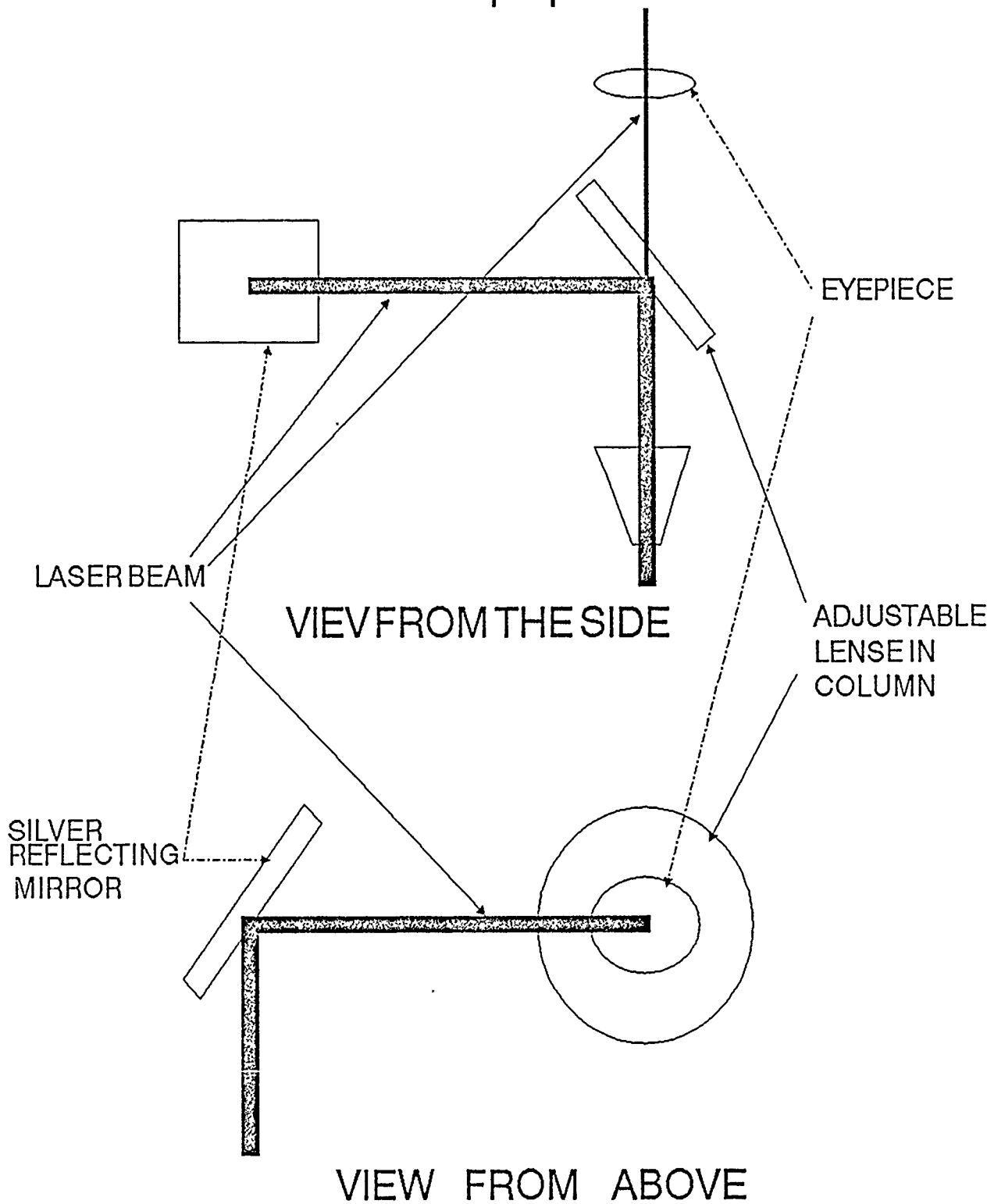
- 1 Spectra Physics Model 124B HeNe Laser
- 1 Newport Electro-Optics Model N10440 Bragg Cell
- 1 Newport Electro-Optics Model N71003 Optics and Stage
- 1 Newport Electro-Optics Model N11440-.6AS Driver
- 3 Newport Corporation Model 45 Damped Rods
- 2 Newport Corporation Model 370-C Rod Clamps
- 2 Newport Corporation Model 360-90 Angle Brackets
- 4 Newport Corporation Model 430-1 Translation Stages
- 1 Newport Corporation Model 300P Mounting Platform
- 1 Newport Corporation Model 32A Platform Fine Positioner
- 1 Newport Corporation Model 280-P5 Jack and Platform
- 1 American Optics Series 3000 Microscope
- 1 American Optics 40X and .55 N.A. Microscope Objective
- American Optics 10X and 20X Eyepieces
- 1 Newport Corporation Model MST 48 Optical Table

- 4 Newport Corporation Model KLA Table Support System
- 1 Newport Corporation Model 471-DM Rotation Stage
- 1 Klinger Model CC1.2 Programmable Stage Controller
- 2 Klinger Model UT-100.25 PP Stage with Encoders
(Micro Controle)
- 1 Tilt Platform Produced In-House

The laser is supported by two damped rods, with one on each end of the laser. Each of these two damped rods holds a rod clamp with a 90 degree angle bracket and two translation stages. This combination allows the laser to be finely adjusted in both the vertical and horizontal directions at both the front and back of the laser. The laser sits on top of the horizontal stage, and is securely affixed to the stage with tie wraps. The Bragg cell is surrounded by focusing optics and a stage. The optics are made by Newport EOS expressly for this model of Bragg cell, and perform the necessary function of focusing the laser beam down into the crystal, and then recollimate the beam when it exits the crystal. The Bragg cell and focusing optics sit on top of the universal mounting platform, which is in turn supported by the third damped rod. The microscope sits on top of a lab jack and platform. This allows the microscope to be adjusted vertically. The microscope is constructed so as to allow a laser beam to enter into the side of the microscope column. The beam is then directed down the column by way of a beam splitter into the microscope objective and onto the DUT. Figure 44 illustrates the optical path of the microscope.

The DUT sits on top of a tilt platform, which is in turn fastened on top of the X-Y micropositioner stage. The stages are attached to the top of a high resolution rotation stage. This arrangement gives the DUT mounting hardware several different axes of movement. All of the above equipment sits on top of an optical table, which is supported by an isolation support system. The electronics test bed sits on the optical table near the DUT. The Bragg cell driver and stage controller also rest on the optical table. Figure 45 shows the layout of the equipment on the optical table.

FIGURE 44
microscope path



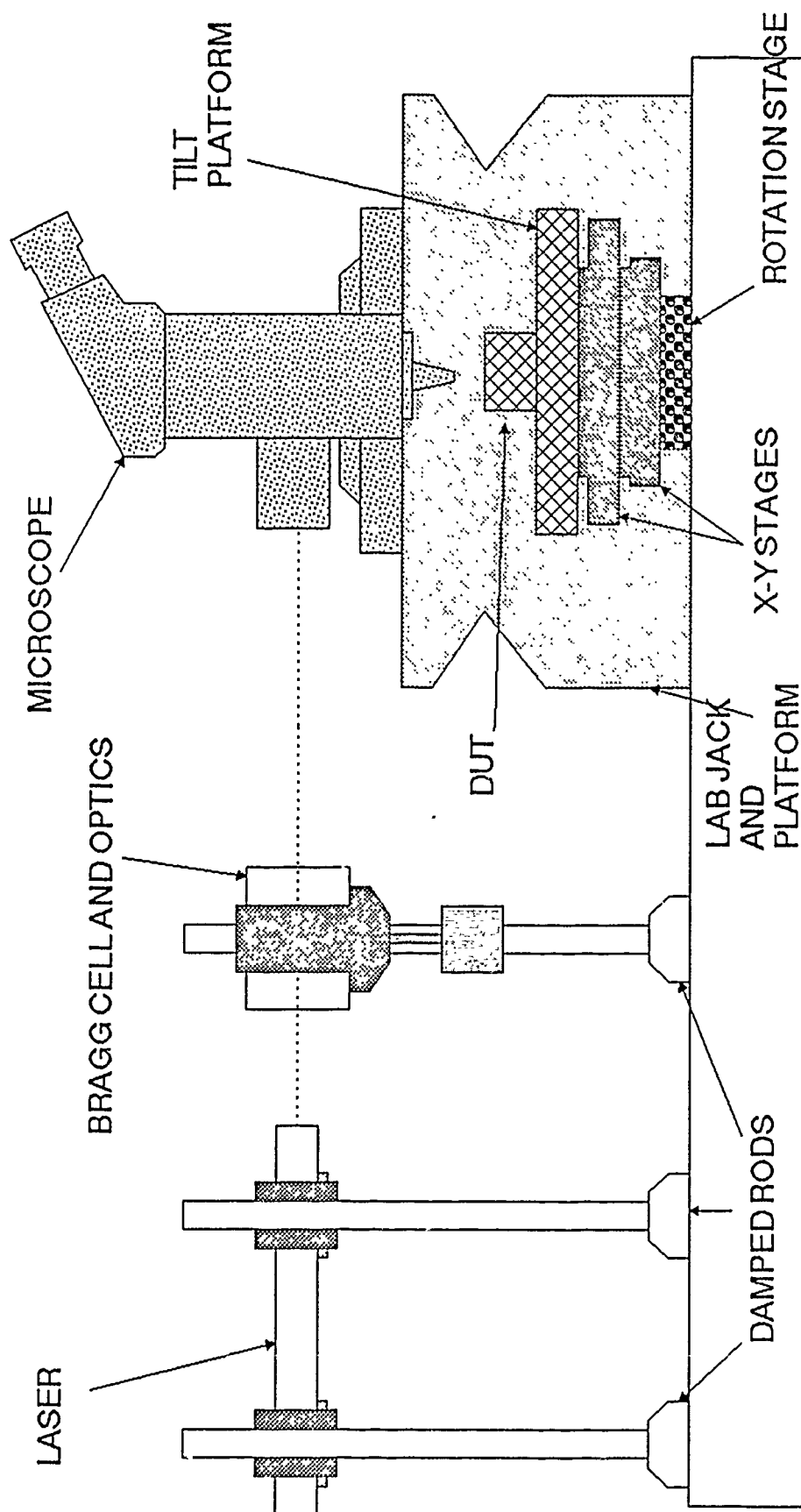


Figure 45. Optical layout of test bench.

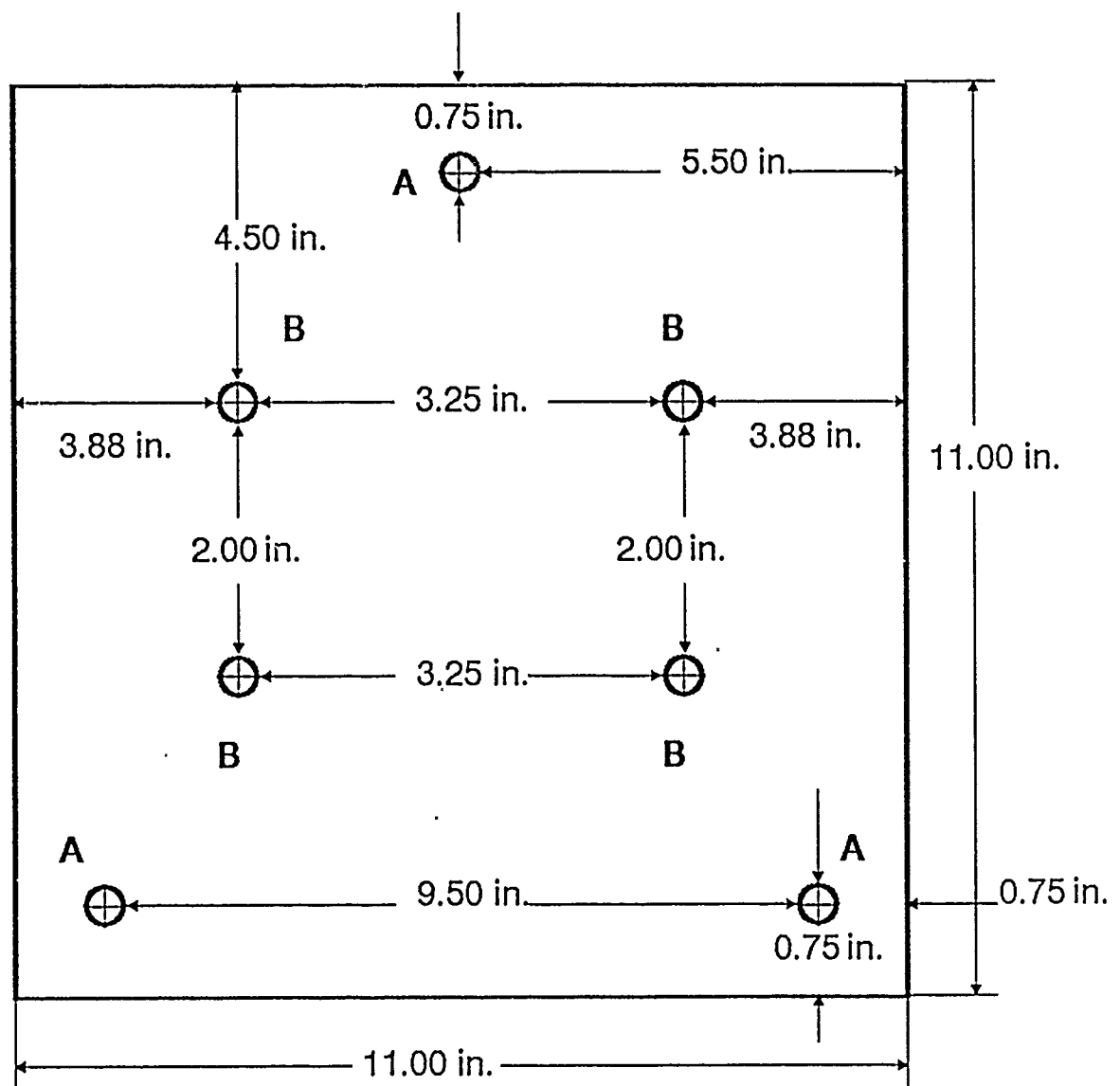


Figure 46 Top Tilt Plate Machining Specification.

A Drilled out to fit 1/4" bolt - do not tap.

B Drilled out to fit 1/8" bolt - do not tap

Plate material - 1/4 inch aluminum.

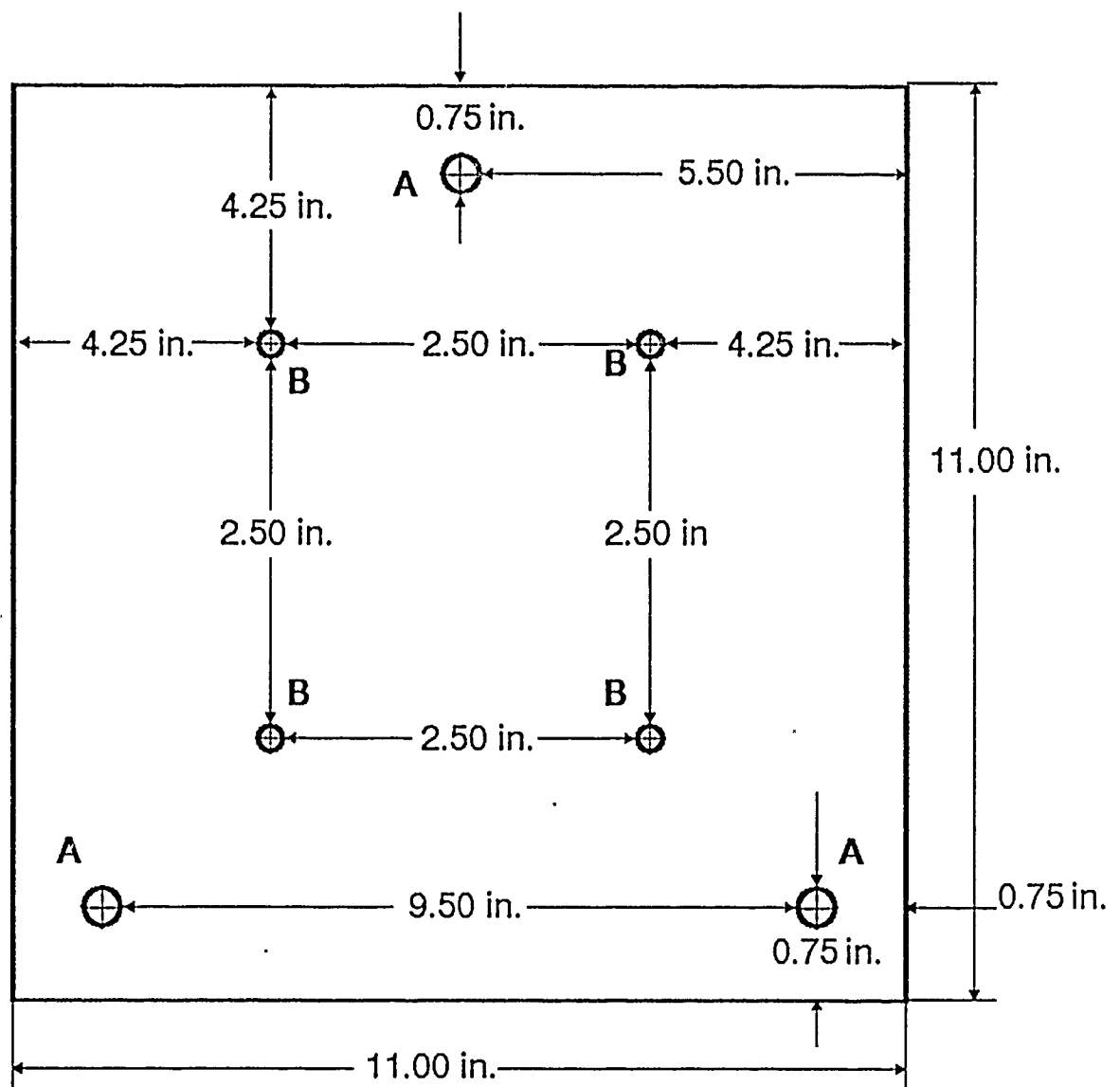


Figure 47 Bottom Tilt Plate Machining Specification.

A Tapped to fit 1/4 - 40 hardware.

B Drilled out to fit 3/16" bolt - do not tap.

Plate material - 1/4 inch aluminum.

The tilt platform used was assembled as follows. Two pieces of 1/4 inch aluminum stock 11 inches square were drilled with the hole patterns shown in figures 46 and 47. The three perimeter holes of the lower plate were tapped to accept 1/4 20 bolts. The other holes of the lower plate were drilled to allow mounting onto the X-Y stages. The upper plate perimeter holes were drilled to allow a 1/4 20 bolt to pass through, but with a minimum of play. The upper plate inner holes were drilled to allow four 10-32 size bolts to pass through with a minimum of play. These four bolts hold a piece of plastic Bakelite (a highly resistive plastic). Attached to the Bakelite is a 14 pin wire wrap socket and four coax cable connectors, which act as a test bed for the DUT.

4.1.2 Characterization of Optics

Spot Size Measurement. The spot size is the diameter of the laser beam waist at the point of focus. The spot size measurement was carried out using a blade and detector technique. To do this a razor blade was affixed across the head of a Newport Corporation Model 835 optical power meter so that half of the head of the meter head was covered by the blade and half of the head was exposed. The meter head was then attached to the stepper motor with the length of the blade edge perpendicular to the direction of a stages travel. The laser was next focused onto the edge of the blade. Next, by moving the stage and measuring the power being received by the meter, it is possible to indirectly measure the spot size. This was possible because our stepper motor driven stage moves in .1 micron increments.

Bragg Cell Characterization. A Bragg cell is a crystal that bends collimated light that passes through it via a Bragg diffraction mechanism. Bragg diffraction is established by launching an acoustic wave across the crystal. This bends or compresses the crystal lattice of the crystal in the vicinity of the acoustic channel, which sets up a diffraction grating. The higher the percentage of light that is diffracted to the first order diffraction lobe, the more efficient the Bragg

cell. The contrast ratio of a Bragg cell is also an important parameter. This is the ratio of power diffracted to the first order diffraction lobe when the acoustic channel is completely on to the power diffracted to the first order diffraction lobe when the cell is completely off. The third parameter of concern with a Bragg Cell is how quickly the acoustic channel can be turned on or off. The rise time and fall time of the power in the first diffracted lobe is a function of the physical parameters of the channel, the speed and power of the cell driver, and the speed of the electronics controlling the cell driver.

Contrast Ratio. The contrast ratio of the Bragg cell used in this study was measured with an optical power meter. The power in the first diffracted lobe was measured with the cell fully on (maximum power in the first diffracted lobe). The Bragg cell was then turned off and the power in the first diffracted lobe was measured. This ratio was 520. It is important to note that only power in the diffracted spot passes through the objective lens of the microscope, and onto the DUT. Stray laser illumination that is detected at the output of the Bragg cell, where the contrast measurement was made, will not be present at the focus of the microscope, so the contrast ratio of the spot at the DUT will be higher than the measured ratio.

Pulse Width. The pulse width measurement was made using a Newport Corporation Model 877 avalanche photodetector and a Tektronix Model 7854 digital oscilloscope. The smallest pulse recorded was 8 nanoseconds. Pulses smaller than this were possible, but the amplitude was reduced due to the finite rise and fall time in the cell driver electronics.

Efficiency. The efficiency of the Bragg cell was measured with a model 835 optical power meter. The cell was turned off and powered down (all of the power of the laser beam was directed through the crystal, with almost no diffraction) and the power of the laser beam was measured. The Bragg cell was then turned completely on (with a maximum amount of the incident laser beam diffracted to the first order diffraction lobe) and the

power of the beam in the first order diffraction lobe was measured. The fraction of the incident beam power found in the first diffraction lobe is the efficiency, which was 47%.

Alignment Techniques. The first step to aligning the optics is to position all of the equipment on the table in their approximate final position. The microscope, laser, and Bragg cell are next secured in their final position. When positioning the microscope it is important to leave enough room beneath the objective to allow placement of the tilt platform assembly, the X-Y stage and the rotation stage, but do not leave so much room that the microscope cannot focus down on the DUT. Next, remove the Bragg cell and align the laser so that the beam travels squarely into the beam input channel of the microscope. If the beam does not enter the microscope perpendicular to the opening of the microscope, the beam will enter the microscope column at twice the angle of incidence to the microscope beam input channel (the first mirror of the scope acts as an optical lever). Next, place the Bragg cell in the path of the laser. It is important to place the Bragg cell close to the laser to minimize the effects of beam divergence of the laser in the focusing optics of the Bragg cell. For optimum efficiency of the Bragg cell, the beam must be focused into the 19 micron wide acoustic column of the crystal. The focusing optics of the cell is capable if this, and there are several iterative steps that must be followed to optimize the Bragg cell alignment.

Bragg Cell Adjustment. First, remove the recollimating lens from the focussing optics stage. Position the focusing lens approximately 25 mm from the center of the crystal, and adjust the angle of the crystal to approximately 4 degrees from perpendicular to the incident laser beam. Focus the beam into the crystal. Next, hook up the cell to the driver and place the driver in the continuous wave operating mode. The system is now ready to focus the beam waist into the acoustic channel. Using the vertical adjustment on the focusing optics stage, move the cell up and down until bragg diffraction is detected. It is a good idea to

place a non-reflective surface about 1 meter from the cell so that the laser beam is easily viewed. A good surface for this purpose is a manilla folder or a highly frosted plastic transparency. The laser spot will diverge greatly from the Bragg cell without the recollimating lens in the focussing optics. At three feet, the laser beam diameter will be approximately six inches. Diffraction will appear as another spot to the right or left of the main spot a distance of approximately 2 beam widths. Using the angular adjustment on the focusing optics, adjust the cell so as to place as much power as possible into the first order diffracted lobe (the lobe closest to the main beam. There will be two of these lobes, one on either side of the main beam, so it is important to choose the lobe that appears to the right of the main beam when the recollimating lens has been removed from the focussing optics.

The next step to adjusting the Bragg cell in it's focusing optics stage is to place an optical power meter in the path of the first order diffracted lobe. Next move the crystal up and down with the vertical adjustment so that maximum power is detected on the power meter. Next, move the crystal's angle with the angle adjustment until maximum power is detected in the power meter. The third adjustment is the horizontal placement of the cell. The closer the beam passes to the transducer on the crystal, the more efficiently the cell will operate. Move the cell with the horizontal adjustment until the main beam is just about to be cut off by the protective shield surrounding the optics. This should maximize the power in the first diffracted lobe. This is also why one wants to use the right lobe, as the left lobe will be cut off by the shield before the main beam is cut off. As a result, the main beam is farther from the transducer. This makes for less efficient Bragg cell operation.

Several iterations of the above alignment technique are generally necessary before the cell is properly aligned. The next step is to move the focusing lens closer and farther from the transducer. The focusing lens will focus the beam into a waist of very small

proportions. For maximum operating efficiency the waist must be focused precisely into the acoustic channel. To do this, the position of the focussing lens must be altered, and then the Bragg cell must be realigned as was described in the above procedure. This is an iterative technique, but it will lead to maximum efficiency from the Bragg cell.

The next step is to install the recollimating lens in the focusing optics. This lens will reconverge the beam after it passes through the Bragg cell. It is also useful in directing the beam into the beam input channel of the microscope. This lens will invert the image of the beams passing through it. Because of this the first diffracted lobe that up until now has appeared on the right of the main beam will now appear on the left.

Microscope Alignment. The microscope alignment, like the Bragg cell alignment, is an iterative process. The first step is to direct the first diffracted beam of the laser into the microscope beam input channel. This is done by moving the recollimating lens of the Bragg cell focusing optics. The first diffracted lobe should be directed slightly below the center of the input channel. An aid for this alignment is to form a piece of paper across the input channel opening, so that the diffracted lobe beam can be easily seen. The beam will be reflected off of a mirror in the input channel onto a mirror in microscope column.

The mirror in the column is mounted to a tilt platform which can be adjusted by moving a pair of nobs on the outside of the microscope column. By adjusting the attitude of this mirror the diffracted beam can be directed down the column. Remove the objective and adjust the mirror until the beam passes through the center of the hole where the objective was. Again, it is good to place manilla folder or some similar non-reflective material a few inches under the microscope column to allow easy viewing of the beam. Replace the objective and adjust the mirror until the diffracted beam passes through the objective. The image of the beam will be clearly visible once the beam is shining through the objective. Next, return to the

recollimating lens on the microscope and move it towards or away from the crystal until the diffracted beam just fills the objective lens. Secure the base of the lens holder to the stage at this time, as this is the optimum distance for the recollimating lens from the crystal.

At this time it is possible to focus the beam down to a 2 micron spot, but the focal point is not necessarily in the center of the region viewable through the microscope. It may even be outside of the region of viewing altogether. By bringing the beam into focus on some surface while looking through the microscope, it is possible to determine where in the field of view of the microscope the spot is being focused. Return to the recollimating lens of the Bragg cell optics. By slightly moving this lens up or down, left or right, the diffracted beam will be brought out of alignment with the objective lens. Re-center the beam by adjusting the position of the mirror in the column, and focus the beam again while looking through the microscope. The position of the focus of the beam will have moved with respect to the field of view of the microscope. It will be closer or farther away from the center of the field of view. Knowing this, it is possible to bring the focus of the microscope into the center of the field of view of the microscope by adjusting the recollimating lens of the Bragg cell focusing optics. It is not necessary to bring the focus of the diffracted beam into the exact center of the field of view (into the crosshairs), because the point of focus of the laser is clearly visible in the field of view.

At this time it would be good to describe some of the optics of the microscope. The mirror used the microscope column was fabricated by the United Lens Company, and was specifically designed to reflect 632 nm light which strikes the mirror at an angle of 45 degrees. Figure 48 shows the transmission of light as a function of frequency for this lens. Light not transmitted is reflected down, and that light that is transmitted strikes the back of the mirror holder. Of the light that is reflected down, if it is focused onto a point, some of that light is reflected directly back up onto the mirror. Approximately 1% of this returning

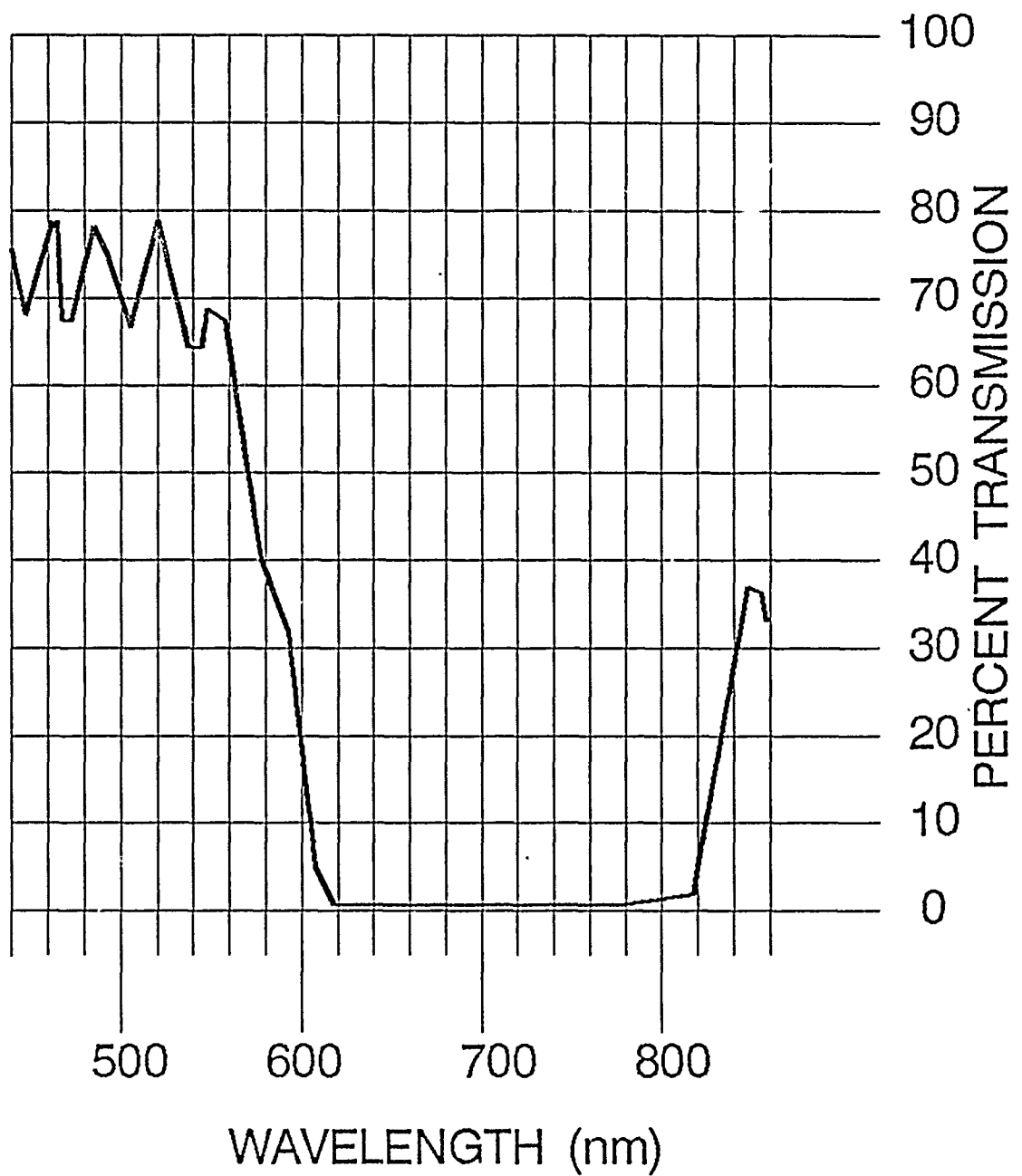


Figure48 Transmission of beamsplitter.

light will pass through the mirror, and that light is visible at the microscope eyepieces. This quantity of light can still be quite bright, but with care it is not bright enough to cause damage to the eyes. As a general rule, when aligning the optical components it is a good idea to filter out as much of the laser power as possible, as a safety precaution. This can be done by placing a polarizer in the path of the beam just after the beam leaves the laser.

Laser Power. The power of the laser beam was measured at several places in the experimental set-up. The first measurement was made at the output of the laser. This was measured to be 22.35 mW. This was measured to be in excess of 27 mW when the laser was first purchased. It is expected that power output of the laser will degrade with time.

The second measurement was made after the beam passed through the recollimating lens of the Bragg cell. The power in the first diffraction lobe was measured to be 10.65 mW. The final measurement was made after the beam came out of the microscope objective. The Power here was measured to be 7.45 mw.

4.1.3 Electrical Components

Two different electronic set ups were used, one for the continuous illumination study and one for the pulsed illumination and capacitance variation studies. The simple device illumination experiment used the HP 4145B semiconductor parameter analyzer described below. The pulsed illumination study and the capacitance variation study used a more complicated set of test bed electronics. This consisted of a fixed timer, a variable timer, an interval timer, an embedded controller, the HP 4145B, and some glue logic. The test bed electronics (with exception of the HP 4145B) are discussed in detail in an appendix. A block diagram of the overall control logic is given in figure 49.

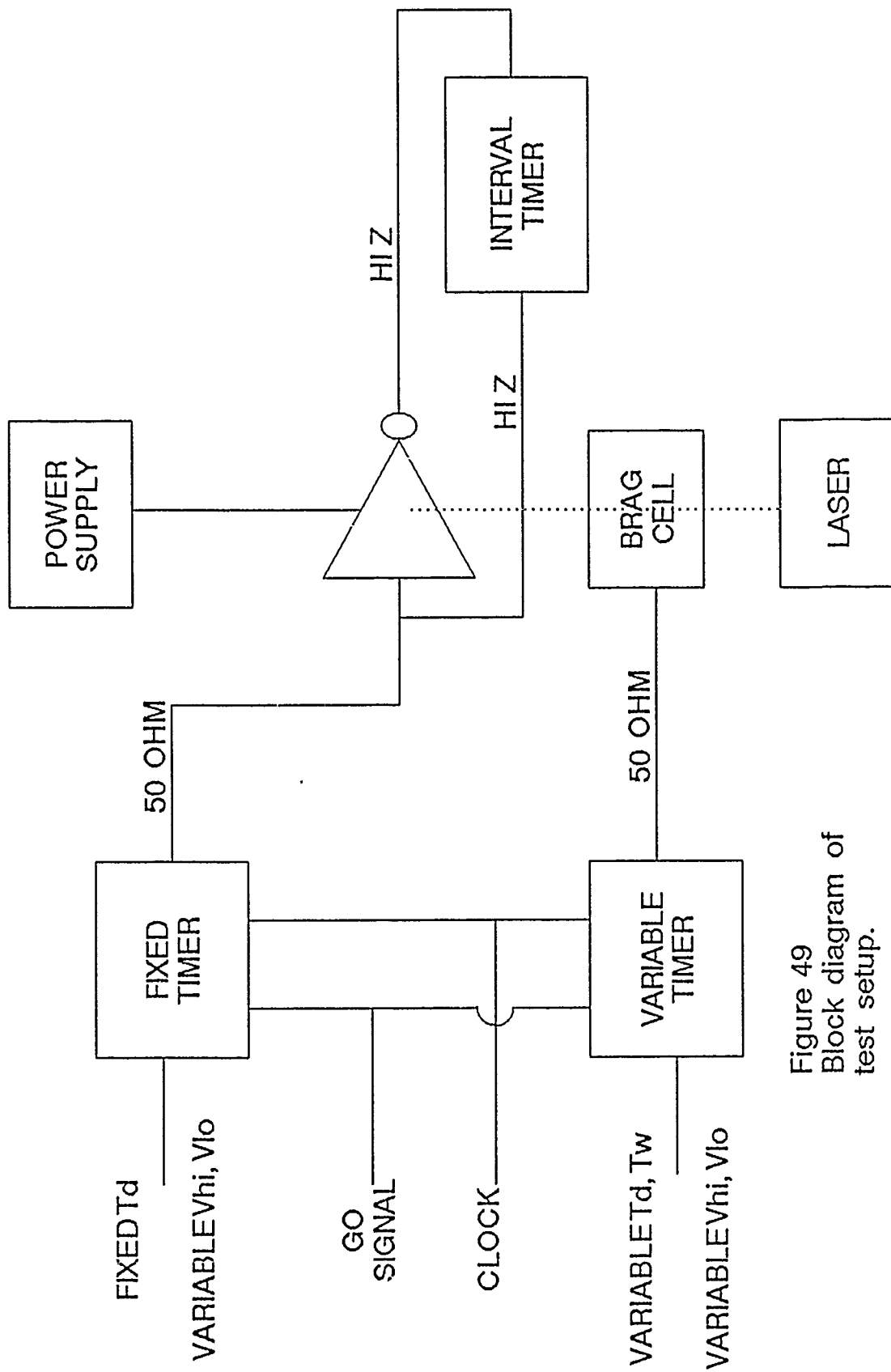


Figure 49
Block diagram of
test setup.

4.1.3.1 Brief Description of Electronics

Controller

The controller to the test bed electronics uses an 80188 MPU and standard peripheral circuitry to locally manage all of the test circuitry. It also has a communications port to interface with an IBM PC to cooperate in the execution of the main test program in the PC.

Master Oscillator

The Master 50MHz clock oscillator needed to properly time all of test electronics. Both the fixed and variable timers need this clock for the simple device test.

Variable Timer

The variable timer enables the Bragg cell to generate a pulse of laser illumination that has programmable delay and width. The long delay accuracy of the timer is due to a digital counter that operates off of the master oscillator, and that can provide a delay of up to 20 milliseconds and a width of 5 microseconds. The resolution of the timer is further increased from the 20 nanosecond limit that the digital counters impose, to a limit of 0.5 nanoseconds, by using a linear ramp circuit to add a trimming delay to the counters. The logic state appearing at the output of the counters can switch between two output voltage levels, both of which are programmable from 0 to 5 volts.

Fixed Timer

The fixed timer gives a signal to the input of the simple device under test. It delays the GO signal by a fixed amount (knowledge of exact value unnecessary), and then switches between two programmable voltage levels in the same way that the variable timer does.

Receive Timer

The receive timer measures the propagation delay of a simple device. The initial circuitry determines by comparators what is a logic zero or logic one input. The logic information then goes to a reckoning circuit that gates a current for the duration of the propagation delay and ramps a voltage from this current. The voltage out of this ramp is proportional to the propagation delay. Another circuit accomplishes the act of determining if the output happened before or after the input. Further circuitry converts this voltage to a digital value to be read by the controller. Along with this is circuitry to control all above, and to alert the controller that the measurement is done. The circuitry in the lower left of the RTMR1 schematic in an appendix generates voltages to be used as input logic level crossing points (to determine if the input voltage is logic "1" or "0".)

HP 4145B Semiconductor Parameter Analyzer

The 4145B Analyzer presents and measures voltages from four input/output test probes. These are connected to the device under test. A test sequence operates the output voltages and currents from these ports and gathers the measurement data (voltage or current) from these ports. The sequence can be entered directly into the 4145B from the console's keyboard, or it can be sent to the 4145B down the GPIB (a instrument communications interface) from a computer. The strong characteristics of the 4145B is that a test sequence can be conveniently executed on the 4145B, and that the measurement ports have special shielding to reduce measurement errors due to leakage currents. The 4145B is used in continuous and pulsed illumination tests, as well as assisting in measuring the output capacitances of the devices. The 4145B is used in totality for the continuous illumination tests, doing all measurements. For the pulsed illumination test, the 4145B provides the supply voltages to the device under test.

Klinger CC1.2 Stage Controller and Micropositioner X-Y Stage

The stage and controller enable automatic laser scanning of device under test. The controller has serial and GPIB ports to allow a computer to control the stage. The accuracy of the stage is 0.2 microns (backlash), and the resolution is 0.1 micron. The stage is used for active device scans, and to switch between N and P channel transistors during pulsed and continuous illumination tests.

4.1.3.2 Characterization of Electronics

Controller - Needs no characterization, except that it must work with the other electronics.

Master Oscillator - Leader frequency counter is used to test frequency. Desired frequency is 50.000 MHz. Actual frequency is 49.99901 MHz. Inaccuracies from such are compensated by software when long delays are encountered.

Variable Timer - Tektronix Oscilloscope reading various delays programmed into the timer.

Delay Aberrations, absolute	
Uncompensated	20 ns max
Compensated (w. fixed timer)	+/- 0.5 ns max
Delay Aberrations, relative	0.5 ns max
Jitter	0.3 ns max
Accuracy, compensated (20 millisecond (MAX) delay)	
50MHz clock	3 ns max
Actual clock	500ns max
Output Voltage Error	+/- 0.4 volt max
Output Rise Time	3.5 ns typ
Output Fall Time	2.5 ns typ

Fixed Timer - Same as variable timer, except aberrations are zero, and jitter is 0.2 ns maximum.

Receive Timer - Test Setup: Variable Timer and Tektronix oscilloscope, referencing delay with the oscilloscope, NOT the variable timer. Calibrated for zero error at small delays (5 nanoseconds), increasing to 1 nanosecond error at 100 nanoseconds, decreasing back to zero at 200 nanoseccnds, increasing to -2 nanoseconds at 500 nanoseconds. Device incapable of resolving propagation delays below 2.5 nanoseconds (the circuit develops singularities of operation at this level), and is limited to a maximum delay of 511 nanoseconds. Input voltage logic resolvency error is 0.3 volts maximum (at 5 nanoseconds).

4.1.4 Test Software

To carry out the continuous illumination tests and the pulse illumination tests, software was required for timer assembly control, measurement operations and result output. The sequence of events for the tests were as follows: ROM based software initializes the timer assembly's intelligent controller and serial link, along with maintaining the measurement protocol. An application on a PC sends measurement parameters to the timer assembly and retrieves the data results via a serial link. This data is then formatted and presented in graphical form.

The ROM based software (which was written by David Lange) performs three general functions, POST operations, serial protocol and measurement operations. A Power On Self Test (POST) first checks the integrity of the 80188 microprocessor, along with other essential control registers of the timer assembly. The system RAM and ROM are checked for proper operation, and upon successful POST, control is shifted over to the application portion of the ROM software. Here the serial protocol initializes the serial link, receives measurement parameters from the PC, and transmits data results back to the PC. All transmitted and received data is verified through the use of sequencing and checksum values. The third portion of the ROM software involves converting the received measurement parameters to register information for the timer assembly, starting the measurement with these values, then retrieving the

data result. A set number of measures (depending on the test) is taken for each group of measurement parameters, and the data results are averaged.

The PC application software controls the test sequence and saves all the results in raw data files. Through a controlled looping structure, the measurement parameters, such as laser pulse width and voltage specs, are sent to the timer assembly. The results sent back are then saved under the appropriate measurement file. A dedicated protocol handles the serial link's sequencing and integrity. Applications for both continuous illumination and the pulse illumination tests follow this procedure. Calibration of the timer assembly is maintained through an application that gives full control over the settings of any of the timer assembly's registers. Two modes of operation will allow either single measurements to be taken, or continuous measurements monitored, all through a simple user interface.

Once the raw data has been retrieved through the PC application software, conversion software (also written by David Lange) is used to create groups of graphical data files. For preliminary data results, where a smaller number of measurements were taken for each point, a running averaging technique was implemented to smooth out the curves.

The source code for the above software is listed in Appendix I.

4.2 Test Procedure

Two test procedures exist. The first procedure is the continuous illumination test procedure, and is used to find β and V_T as per section 2. The second test is the pulsed illumination test, and this tests the inverter's response to a pulse signal.

4.2.1 Continuous Illumination Study

In this test the DUT was placed in the test bed and illuminated with various levels of continuous illumination while at varying supply voltages. The

purpose of this test was to determine how a simple CMOS gate behaves while under continuous illumination from a HeNe laser.

4.2.1.1 Experimental Procedures

STEP ONE: The DUT will be connected to the HP4145B semiconductor parameter analyzer while in the test bed. With no illumination of the device, threshold voltages and the supply current will be measured as the DUT is caused to make a transition of states. The supply voltage be set at 2 volts. The input voltage will ramp from 0 volts to the supply voltage.

STEP TWO: Step two is a repeat of step one, except that the DUT supply voltage is increased from two volts to 2.5 volts. This step is then repeated six times, each time increasing the supply voltage one half of a volt until the device is tested at five volts.

STEP THREE: In step three, the steps above will then be repeated several times, each time incrementing the test station's laser power level output by 20% of the station's maximum output power level until the device is tested at the 100% power level.

STEP FOUR: In step four, the above steps will be repeated, except that the p-channel drain will be illuminated rather than the n-channel drain.

Results. The plots in Appendix I under "Continuous Illumination" give the supply current drawn vs the input voltage of the DUT and the output vs the input of the DUT. The β term may be given as K_p .

4.2.2 Pulsed Illumination Study

The pulsed illumination study was carried out with the DUT illuminated by a pulsed HeNe laser. The intensity and duration of the pulse, as well as the supply voltage of the DUT was varied. Both the n and p-channel were illuminated. The propagation delay was examined for both rising and falling inputs, and the temporal displacement of the laser pulse with respect to the rising or falling input was varied. The propagation delay was the only parameter measured during this study.

4.2.2.1 Experimental Procedure

STEP ONE: The laser of the test station is focused on the n-channel drain of the DUT. The laser is set for a 10 ns. pulse of maximum possible intensity. The supply voltage is set at 5V. The DUT is made to change state with an input going from low to high, and with the laser pulse beginning 50 ns. before the beginning of the change of state of the DUT. The propagation delay of this transition will be measured. The procedure will be repeated, with the laser pulse occurring 48 ns. before the beginning of the change of state. The procedure will continue like this, each time changing the time that the laser pulse illuminates the DUT. The pulse will eventually occur at the same time that the change of state transition occurs, and then after the start of the change of state of the DUT. Each time, the propagation delay will be measured.

STEP TWO: Step two is a repeat of step one, but with an increased pulse width. The pulse will be increased to 20 ns. and step one repeated, and then increased to 30 ns. and step one repeated again. This procedure will be repeated over and over, each time increasing the pulse width by 10 ns. until a pulse width of 100 ns. is reached.

STEP THREE: Step three is a variation of the steps above but with a decrease in the intensity of the laser pulse from 100% of maximum for the pulse to 80% of maximum intensity for the pulse. This will then be repeated over and over, each time decreasing the intensity of the pulse of light by 20% until after the device has been tested with no laser illumination intensity at all.

STEP FOUR: Step four is a repeat of the steps above, but with a falling input instead of a rising input.

STEP FIVE: Step five is a repeat of steps one through four, but with a decrease in the supply voltage from 5 volts to 4 volts. This will then be repeated several

times, each time decreasing the supply voltage by 1 volt increments until the DUT has been tested with a supply voltage of 2 volts.

STEP SIX: step six is a repeat of the steps above, but with the p-channel active area of the transistor illuminated instead of the n-channel active area.

Results. The graphs in Appendix I under "Pulsed Illumination Study" are composite graphs of the data taken in the simple device test. The heading of each graph describes the conditions under which the data for each graph was taken. The heading of each graph provides which active area is being illuminated, the supply voltage of the test, whether the input for the test is rising or falling, and the intensity of the laser beam.

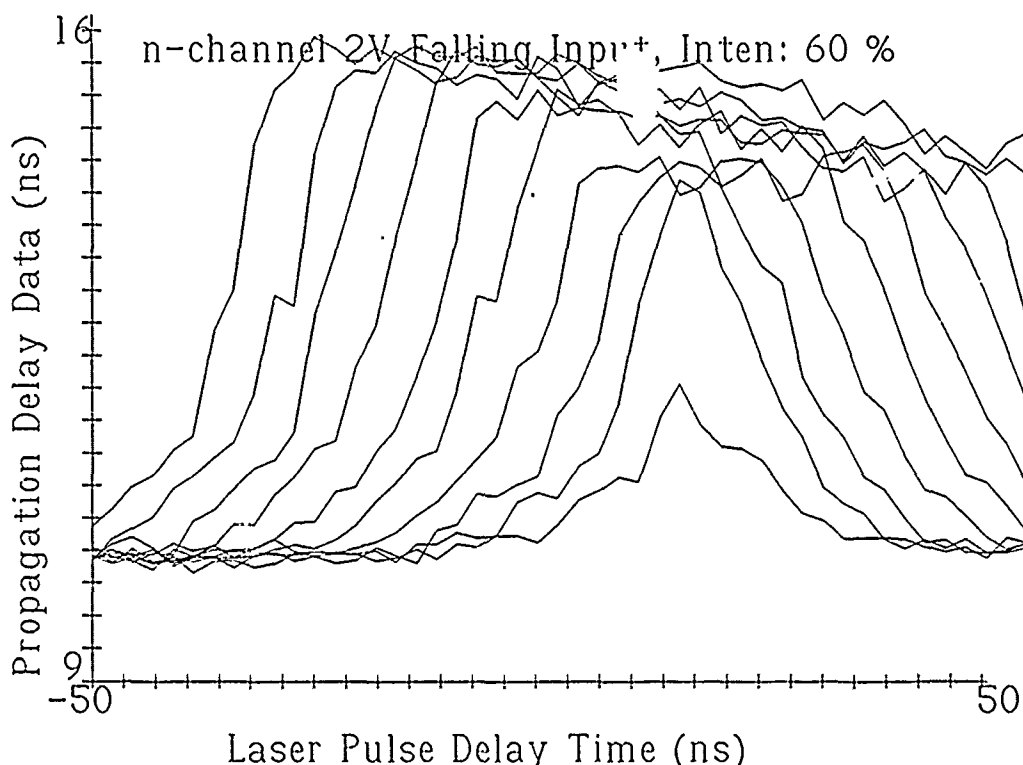


Figure 50 Proper propagation delay change.

The intensity percentage is the percentage of the maximum beam power that was used in the test in question. The first set of graphs show the n-channel illuminated, and the second show the p-channel illuminated. All of this information remains the same

throughout each graph. Each of the graphs contain several traces. These traces correspond to beam intensities of various pulse widths. For the example of figure 50 and 51, the curves corresponding to 100 ns. laser pulse widths are toward the top of the graph, and the curves corresponding to 10 ns. pulse widths are at the bottom. The propagation delay of the inverter pair is shown in the vertical axis, with larger propagation delays seen as traces appearing higher on the graph. The horizontal axis shows the time at which the center of the laser pulse occurs with respect to the occurrence of the change in the input of the inverter.

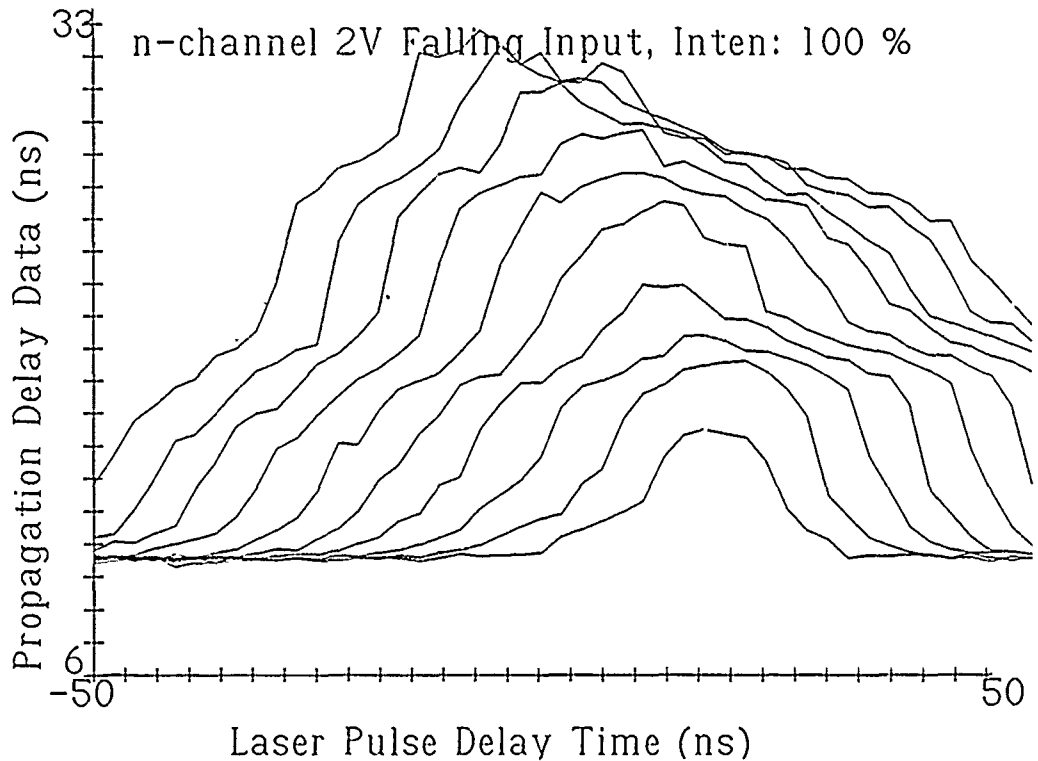


Figure 51 Laser too powerful.

In Figure 50 on the previous page, the propagation delay has been increased by the use of laser illumination from about 10.5ns to 15ns. Notice the nearly flat top. For very wide pulses, the propagation delay is dependant only on laser illumination and is independent of pulse width. This

delay will be used to calculate the delay versus intensity for this inverter. This diagram best fits the simulation of figure 30.

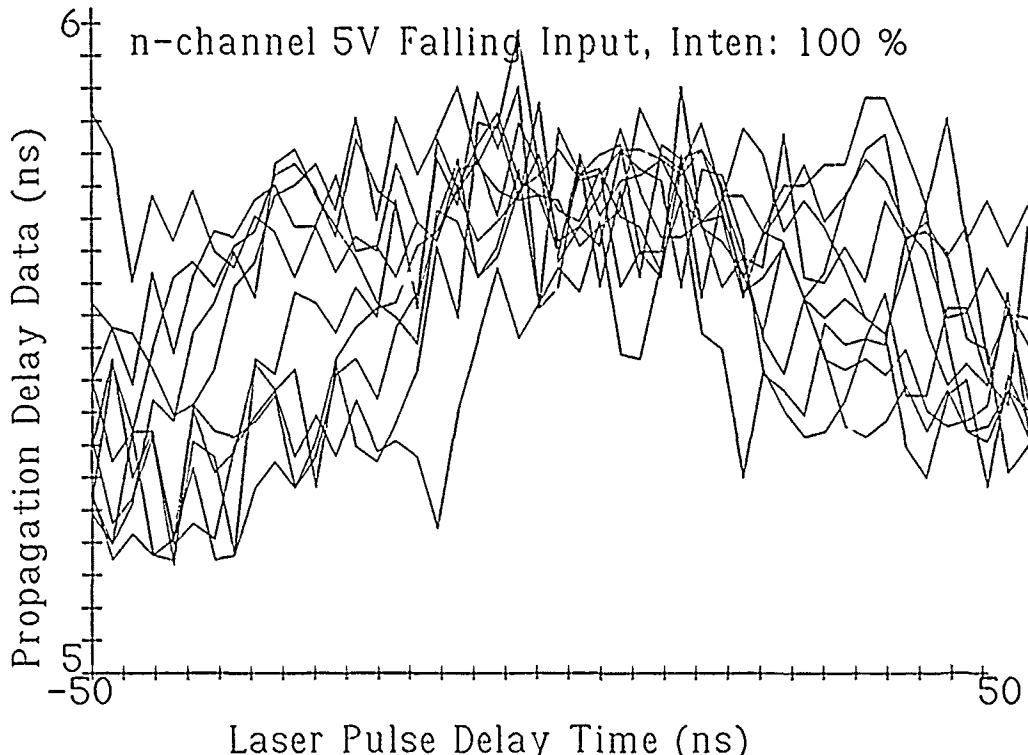


Figure 52 Five volt test. Laser very weak in comparison.

In Figure 51, the output does not have a distinct flat top, as the laser is very powerful in this test case. Although the laser does not outright cause the inverter to hold state in this case, the propagation delay still cannot be accurately determined. In this case, however, a maximum propagation delay of 33 nanoseconds is not far off.

Notice that the two previous figures showed the device operating at a 2 volt supply voltage. This one (Figure 52) is operating at 5 volts. Notice that the laser has much less effect at this voltage (about 0.7ns). This presents a problem for the complex device at 5 volts, as the laser will have a narrower margin for propagation delay control. Although logic

state change did not happen on this device, as geometries were large, it would more likely happen on a complex device, with its smaller geometries.

Also notice the noise. This noise is from test equipment noise and device thermal variations. Gross statistics, such as 100 sample averages, are already used to lessen the noise effects on the outcome, but the ability for the type of circuitry used (see an appendix for further details) to resolve 10 picosecond differences has been grossly overestimated.

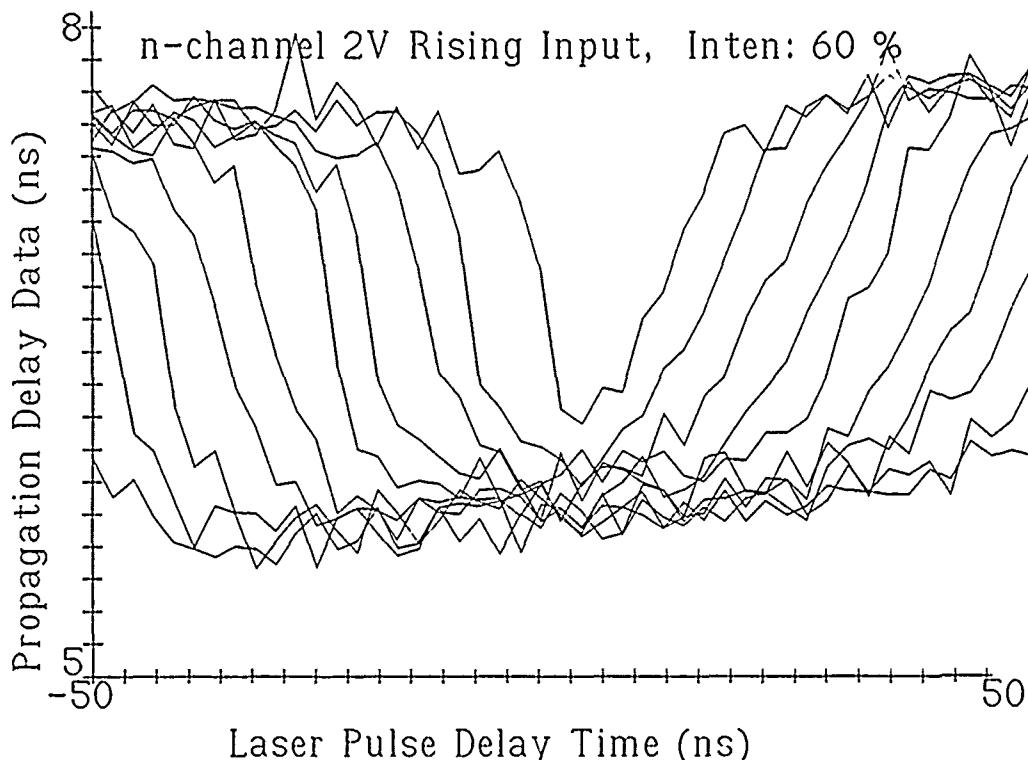


Figure 53 Laser lowering propagation delay.

Although this report has mostly explained a laser increasing the propagation delay, just the opposite can also happen. Figure 53 shows how a laser can decrease the propagation delay of an inverter (from 7.5ns to 5.5ns). The upper curve in this curve set is for a pulse width of 10 ns. and the bottom curve is for a pulse width of 100 ns.

Finally, the data from several figures above are matched to the delay versus intensity curve for best fit of curvature without modifying the curvature of the data or simulations. This shows that the models and the simulations do fit well with the data.

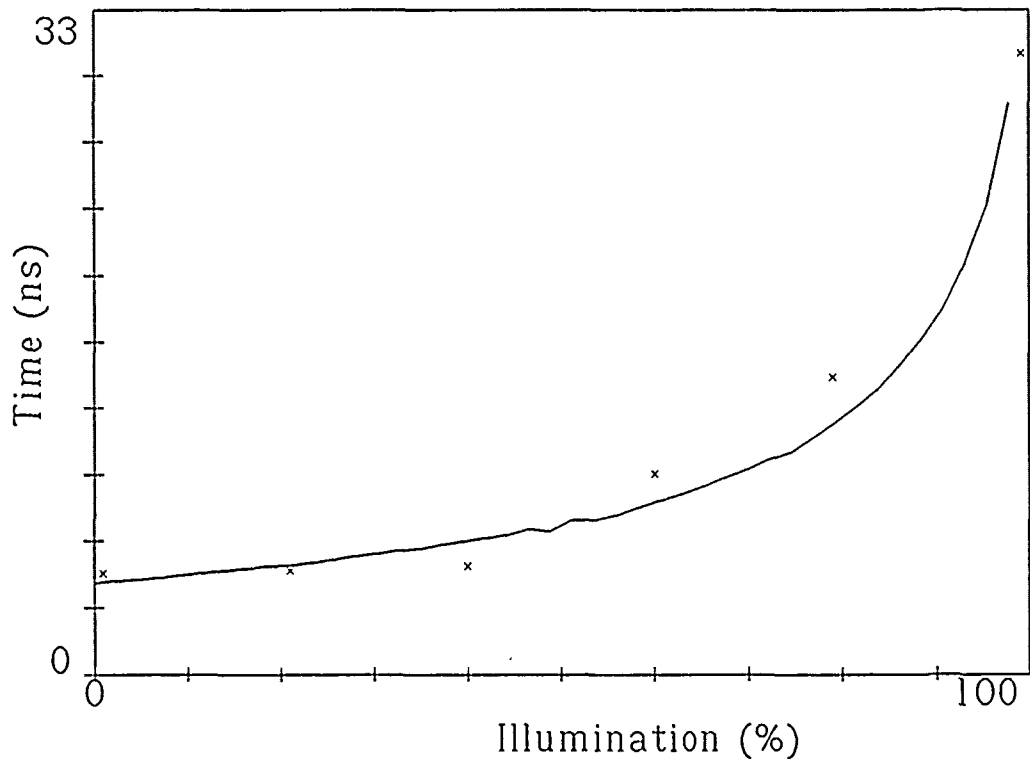


Figure 54 Delay versus intensity.

The X's in Figure 54 are from 2 volt supply data, with the variables such as V_T and β between the measurements and simulations the same. The line is a simulated data curve with parameters from the measurements. The bumpiness in the curve came from a resolution problem in the simulation that the other curve in Chapter 4 did not have. Nonetheless, the two curves are close to being identical with respect to curvature.

5 Complex Device Test

5.1 Overview

The purpose of the experimentation was to determine whether or not the proposed technique for measuring timing margin was feasible. To be useful in an industrial setting, the technique must be applicable to complex semiconductor devices exercised under normal operating conditions. For this reason the test device was chosen to be quite complex (a Harris 80C88 microprocessor was tested, and the operating environment was chosen to meet standard TTL specifications (5V supply, room temperature, etc.)).

The experimentation involved identifying and illuminating transistors with a helium-neon laser in such a way as to increase the propagation delay of the illuminated gate. Increased propagation delay was detected as a decreased maximum operating frequency of the device under test (DUT). As the layout of the DUT was not known to us, and automated testing was desirable, node selection was carried out through a process of semi-random stage movement followed by illumination of the DUT. Nodes with critical timing were identified by searching for logical failures at the output of the DUT.

The laser was directed onto the DUT through a microscope whose optics generated a nearly diffraction limited spot size. This small spot (on the order of two microns) insured that only one transistor was being illuminated at a time. The microscope facilitated visual siting of the DUT to allow for manual focussing of the laser beam, and alignment of the DUT.

Control of the laser beam was carried out through the use of a Bragg cell. A Bragg cell is a crystal which, when an electrical voltage is applied across it, distorts in such a way as to induce Bragg diffraction of a properly oriented laser beam. Modulation of the voltage across the Bragg cell results in modulation of the magnitude and duration of the beam diffraction. The Bragg cell enabled laser beam pulses of chosen duration and intensity to be diffracted into the optical path of the microscope under external control. Pulses as short as 10 ns were generated, and continuous illumination of the DUT was

available.

The orientation and movement of the DUT was facilitated by a complex stage arrangement. Rotational movement was accomplished through the use of a rotation stage. Movement in the X and Y direction (perpendicular to the laser beam) was accomplished through a pair of translation stages equipped with stepper motors capable of external control. Translation occurred in 0.1 micron steps. Variations in the Phi direction (parallel to the laser beam) were leveled using a tilt stage. The tilt stage was necessary to insure that translational movement did not alter the focus of the laser beam on the DUT. Once the DUT was properly aligned, only movement in the X and Y direction was necessary to view the DUT.

The Bragg Cell, the X-Y stage movement, the data storage, and the vector input to and data capture from the DUT were all operated under computer control. Several pieces of custom electronics were fabricated as part of the test equipment. These consisted of a controller, a master oscillator, a variable timer, capture memory circuitry, a sequencer, and a variable frequency clock generator.

5.2 Device Under Test

5.2.1 Device Description

The test device is the Harris 80C88 microprocessor. This is a CMOS version of the Intel 8088 microprocessor that Harris produces under an agreement with Intel. The 8088 is a third generation microprocessor with a one megabyte (20 bit) memory address space, a 64 kilobyte I/O address space and an external eight bit multiplexed data bus. Two processing units, the Execution Unit (EU) and the Bus Interface Unit (BIU) operate in parallel. The BIU fetches instructions and places them into a four byte queue, while the EU simultaneously executes them.

The EU executes instructions in the queue with the help of a sixteen bit Arithmetic Logic Unit (ALU), eight 16 bit general purpose registers and six 1 bit status flags. The general purpose registers can be used as word or byte registers, and have additional uses when coupled with certain instructions. The EU provides all data and addresses to the BIU. The BIU includes segment

and instruction registers used to create the 20 bit address, and a 4 byte instruction prefetch queue. The BIU is responsible for transferring data to and from the EU.

The physical 1 megabyte memory address space of the 8088 is divided into 64 kilobyte logical segments. Most of the EU's instructions operate within a logical segment, while the location of this 64 kilobyte segment inside the entire 1 megabyte address space is held in a segment register. Up to four logical segments can be accessed at one time through the four segment registers CS, SS, DS and ES. The CS register holds the code segment location, the SS holds the stack segment location, the DS and ES generally point to data spaces.

The instruction set of the 8088 includes program transfer instructions, data transfer instructions, string instructions, arithmetic instructions, bit manipulation instructions and processor control instructions. Most all of the instructions can operate with both byte and word data, and work with register or direct transfer, along with several memory addressing modes. The modes supported are direct, register indirect, base, indexed, based indexed and string addressed.

The 8088 package used for device testing was a forty pin dual in line package (DIP) which operates off of a five volt power supply. The EU and BIU timing is based on an external clock signal which is internally divided for a thirty-three percent duty cycle. An external reset pin is used to initialize the processor, and begin execution at a specific location.

5.2.2 Test Vector

To exercise the device under test, a test vector is executed. The results of this execution are saved into logical capture RAM, and examined later by the supervisor software. The test vector set consists of startup and diagnostic code to validate internal operations, memory addressing, I/O operations and arithmetic operations. Once an inconsistency is encountered, a failure message is sent to the capture RAM. Successful completion results in a passing

message. If the capture RAM contains no message, failure is assumed. The controlling software uses the message in the capture RAM to determine whether or not the device operated correctly.

A device test sequence is initiated when the device is given a reset signal. After the reset, the device begins to execute a series of tests designed to exercise the chip. The test sequence is initiated by disabling the interrupt structure, preventing any spurious exceptions. The device's internal flags and flag based conditional transfers are then tested. A complete internal register set test, which swaps values and performs logical and conditional tests, follows. The arithmetic unit of the device is then tested with a series of addition and subtraction routines. If any of these tests fail, a FAIL_CODE is output to the capture RAM. Upon the successful completion of the device test sequence, the OK_CODE message is output to capture RAM.

A full description of the test vector can be found in an appendix.

5.3 Experimental Set-up

5.3.1 Optical Components

The primary optical device used in the the experimentation was a Spectra Physics model 124B helium neon laser. This laser emits 632.8 nanometer light with a power rated to at least 15 milliwatts. The laser was supported by a pair of damped rods. Each damped rod held a 90 degree angle bracket and two translation stages. This arrangement allowed for precise positioning of the laser. The laser was found to be too powerful to use at maximum intensity, as it caused chip damage on more than one occasion. To reduce the chance of latch up, the intensity of the laser was attenuated through the use of a polarized filter. The intensity varied during the test procedures from approximately 900 microwatts to 600 microwatts.

The beam of the laser was directed into a Bragg cell and focussing optics manufactured by the Newport Electro-Optics Corporation. The Bragg Cell required that the beam waist passing through the acoustically altered diffraction channel be no larger than 19 microns

in diameter. Further, the angle and location of the laser beam incident on the diffraction crystal must be precisely aligned. To meet these requirements, Newport supplies a stage with focussing and recollimating optics and three degrees of movement. Proper alignment techniques will allow a fraction of the laser beam to be diffracted into the optical laser path of a microscope by the Bragg cell. The voltage across the Bragg cell, and thus the diffraction induced by the cell, is provided by a Bragg cell driver which accepts a 0 to 1 volt control signal as an input, with zero volts corresponding to no diffraction and one volt corresponding to maximum diffraction.

Bragg cells are characterized by the efficiency of the cell, the cell's rise and fall time, and its contrast ratio. The efficiency is defined as the fraction of the incident laser beam that can be shifted into the first diffraction lobe. This efficiency is dependent upon the quality of the alignment. The typical efficiency attained in the experiment was 53 percent. The rise time of the cell is defined as the time required to shift from 10 to 90 percent of the power available in the first diffracted lobe into that lobe. The cell used in the experiment had a rise time of 4 nanoseconds and a fall time of 3 nanoseconds.

The contrast ratio is defined as the ratio of the power in the first diffracted lobe when maximum diffraction is occurring divided by the power in the first diffracted lobe when minimum diffraction is occurring. This ratio was measured to be 520/1. This measurement was made with an optical power meter. The contrast ratio is an important value, as a small fraction of the laser beam is always leaking through the optical path onto the DUT. This leakage must be kept as small as possible. The primary source of noise is voltage leakage in the Bragg cell driver. Because of this, attenuation of the maximum laser beam power is carried out with polarizers rather than the Bragg cell.

The laser beam is directed out of the first diffracted lobe of the Bragg cell into the microscope. The microscope used was an American Optics series 3000 microscope. This microscope has two optical paths, one

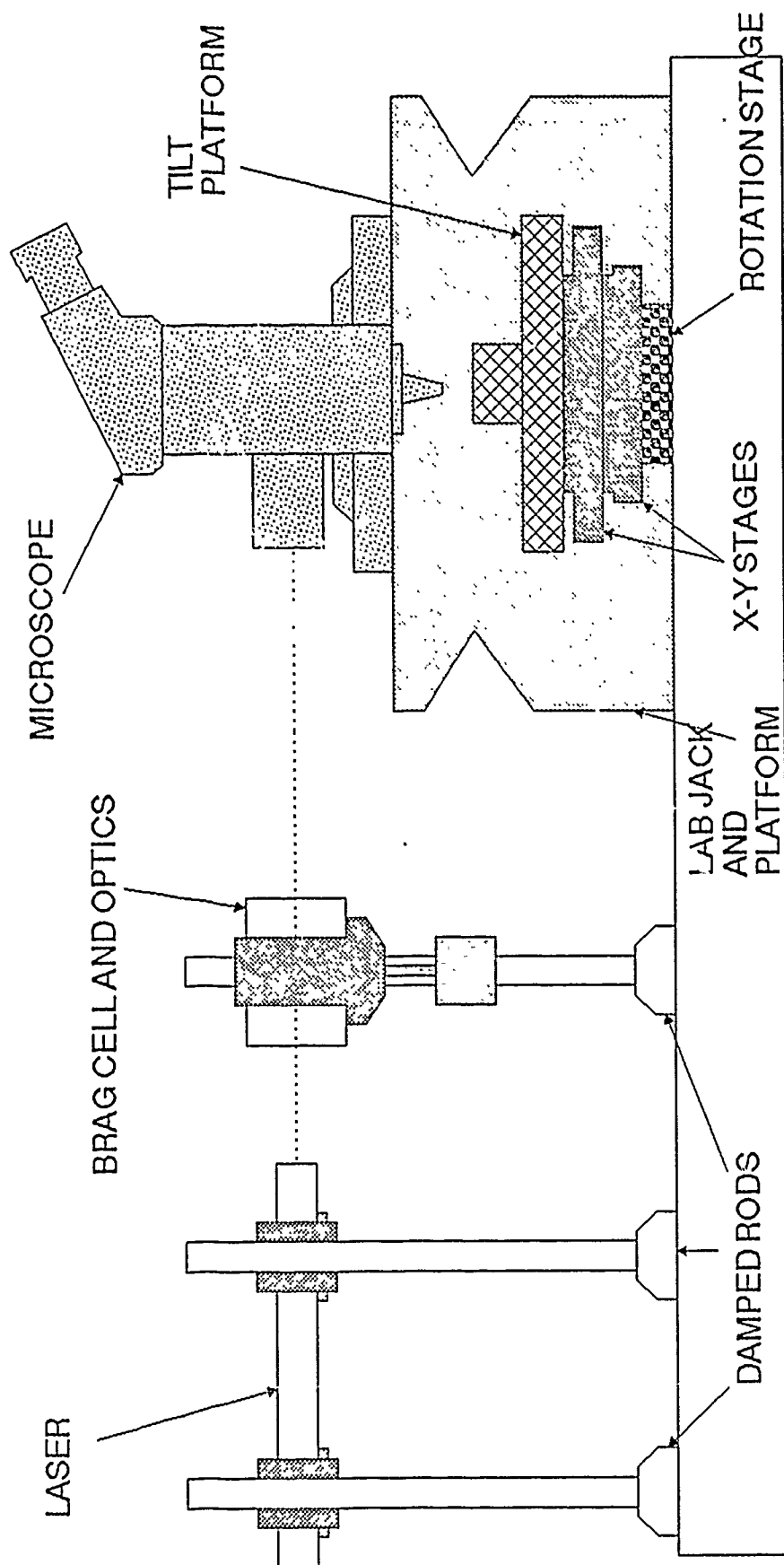


FIGURE 55: THE OPTICAL COMPONENT LAYOUT

for the incident laser beam and one for viewing the object of the laser illumination. The laser beam entering the first optical path of the microscope is deflected ninety degrees by a silver coated mirror towards the center of the microscope column. Upon entering the microscope column, the beam is deflected down the column into the microscope objective by another mirror. The second mirror is a frequency specific reflector, and allows all but red light to pass through it. The first optical path is arranged in such a way as to allow movement of the microscope in a plane perpendicular to the column without affecting the focus of the microscope. The second optical path of the microscope allows viewing through the frequency specific mirror and the objective onto the focal point of the microscope, and so provides for visual alignment of the laser beam.

The microscope was fixed on top of a Newport corporation lab jack and platform assembly with a vertical positioning capability varying from 8.5 inches to 11.5 inches.

The DUT is mounted on top of a four stage assembly. The stages have been arranged to allow for a limited freedom of movement in every axis. The stages are arranged with a tilt stage mounted on top of two orthogonal translation stages, which are mounted mounted on top of a rotation stage.

The tilt stage holds the DUT and the electronics surrounding the DUT. It consists of two aluminum plates eleven inches square and 0.25 inches thick. These plates are held apart by three springs. Their spacing is controlled by three $\frac{1}{4}$ -20 bolts coaxial with the springs and arranged to allow small angle adjustments of the upper plate with respect to the lower plate (three points determine a plane.) Figure 57 and Figure 58 depict the upper and lower plates.

The translation stages are Klinger UT-100's. Their position is controlled by stepper motors and a stepper motor driver. The driver allows stage movement in .1 micron steps.

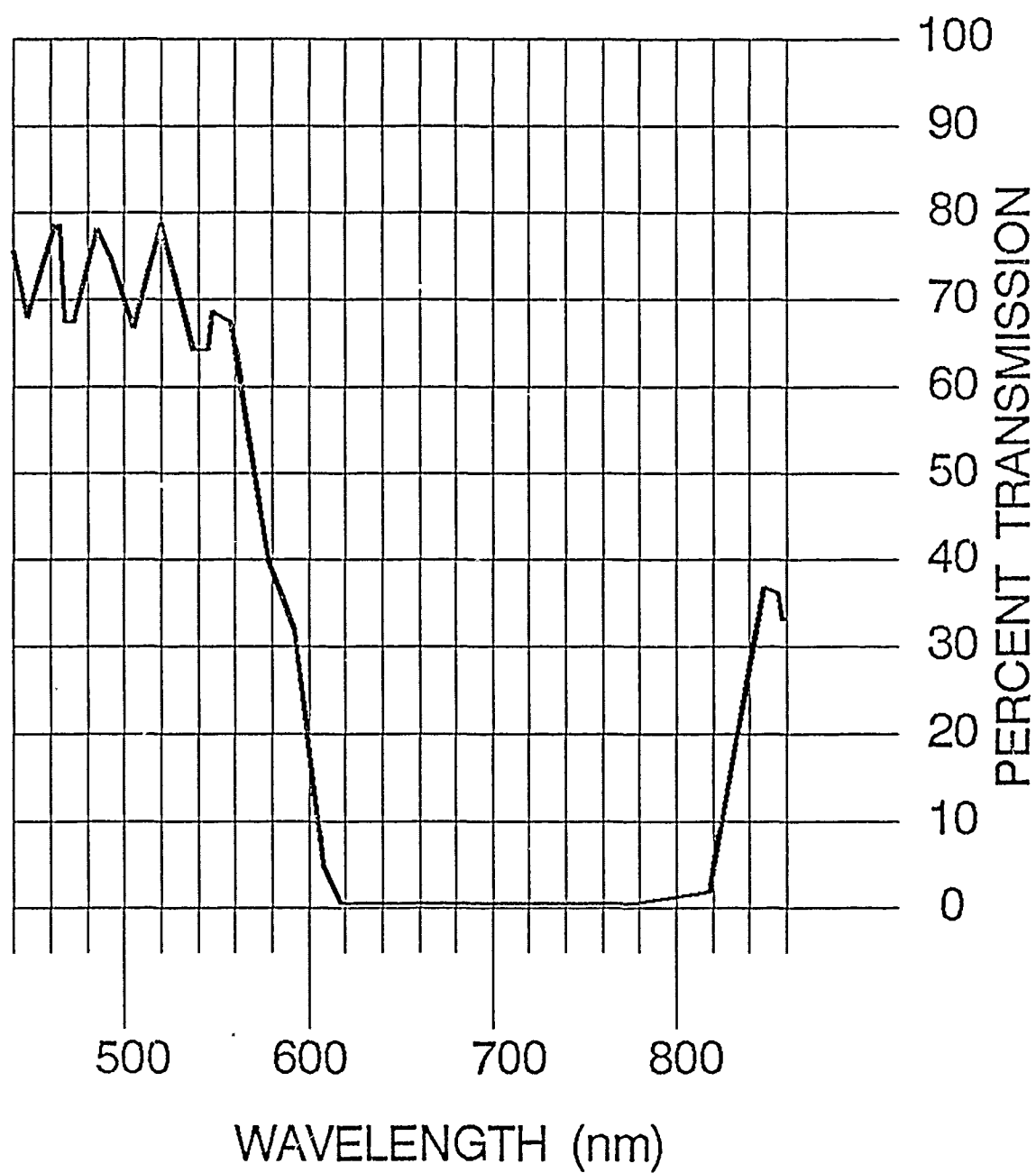
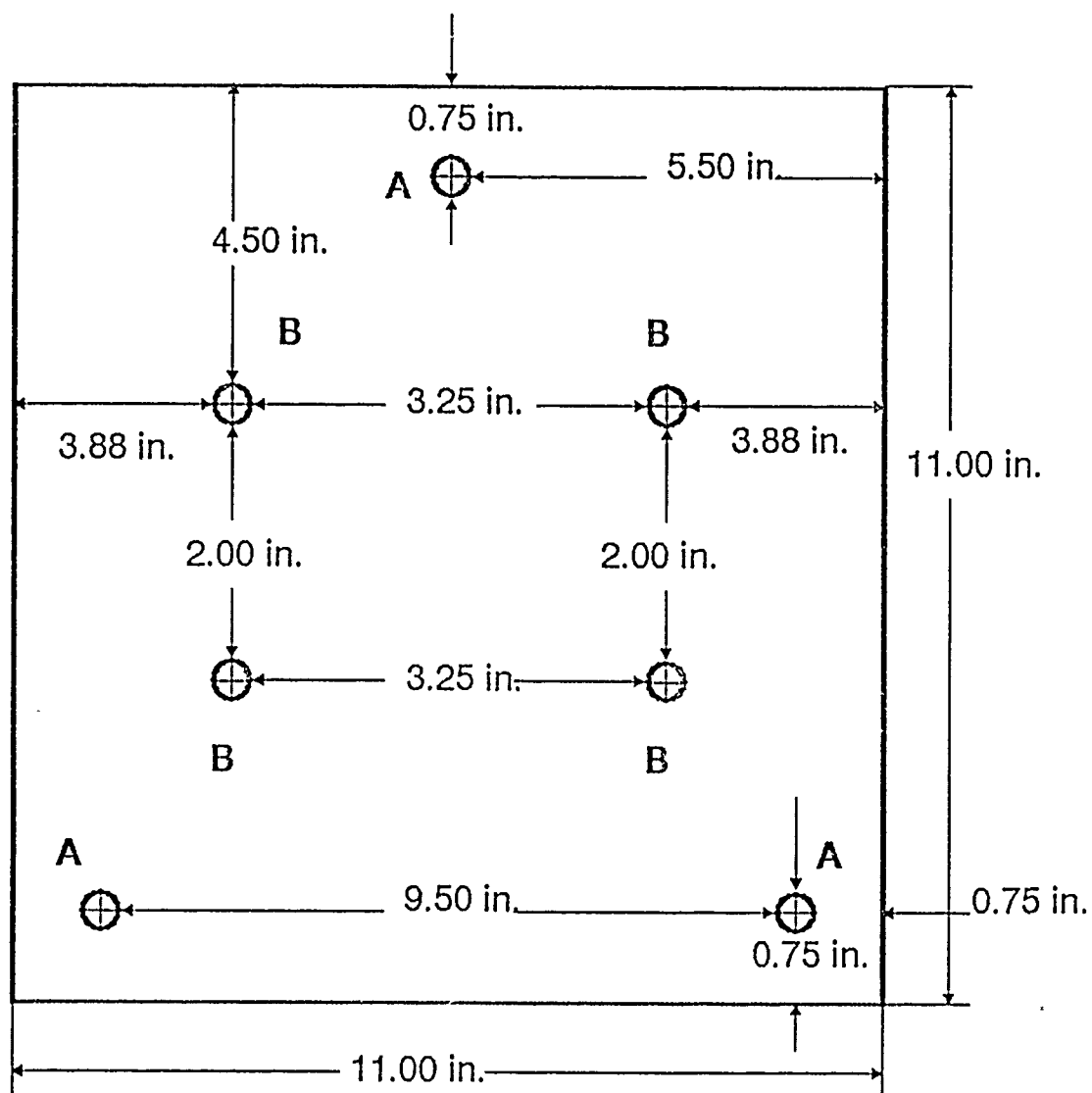


FIGURE 56: FREQUENCY SPECIFIC MIRROR TRANSMISSION

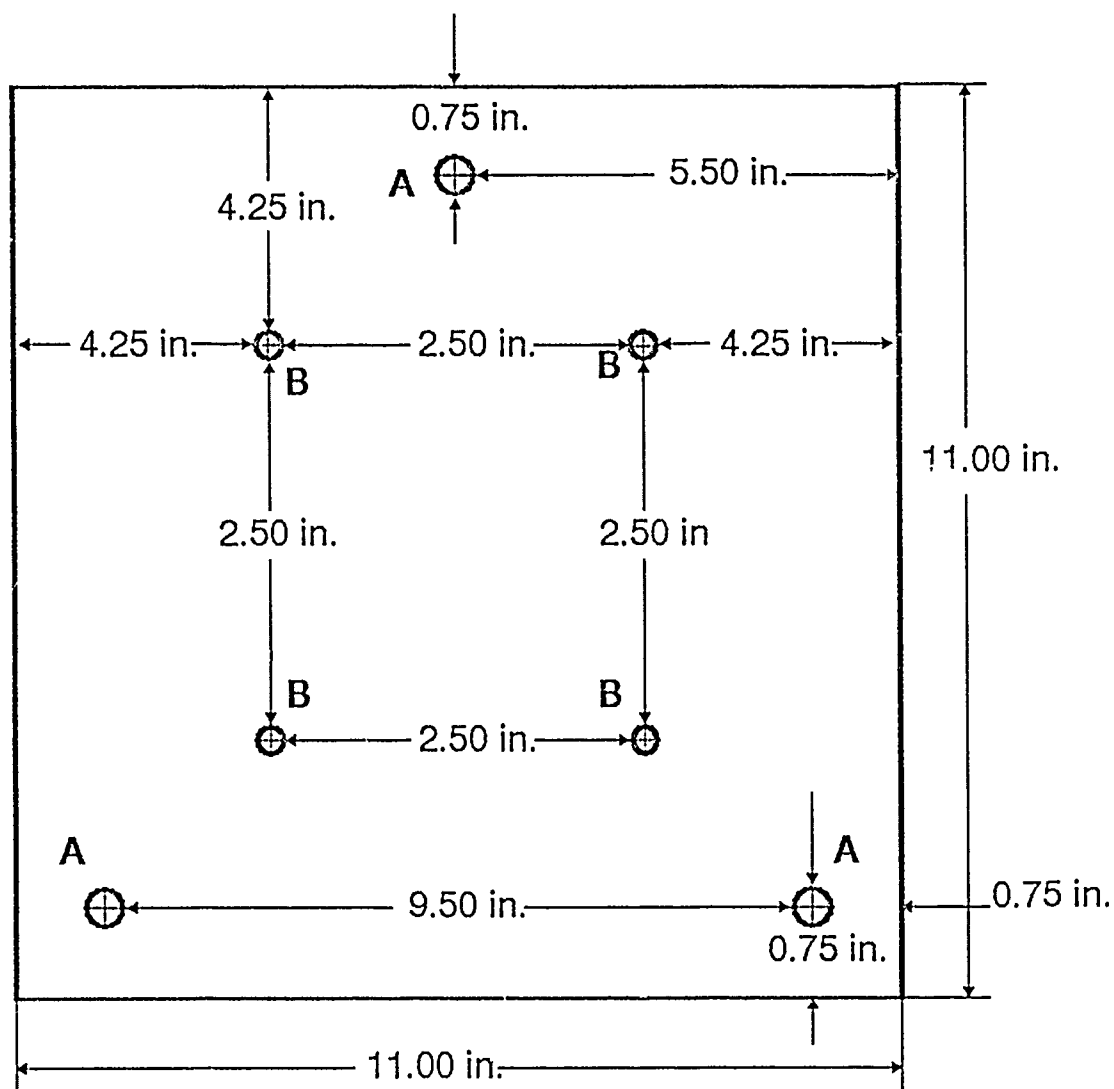


A Drilled out to fit 1/4" bolt - do not tap.

B Drilled out to fit 1/8" bolt - do not tap

Plate material - 1/4 inch aluminum.

FIGURE 57: UPPER PLATE LAYOUT



A Tapped to fit 1/4 - 40 hardware.

B Drilled out to fit 3/16" bolt - do not tap.

Plate material - 1/4 inch aluminum.

FIGURE 58: LOWER PLATE LAYOUT

The rotation stage is a Newport corporation model 471 stage with .3 arc-second resolution, a three arc-second backlash and a three arc second repeatability. This is the bottom stage, and is firmly attached to the optical table.

5.3.2 Electrical Components

The electrical components consisted of several off the shelf and custom electrical systems used in the experimentation. The off the shelf items consisted of a stepper motor controller, a Bragg cell driver, and an IBM PC. The custom electronics consisted of an embedded controller, a master clock, a variable delay timer, a variable frequency square wave generator, a sequencer, and a vector generator and capture board. Each of these items will be detailed below. For a more complete description of the electrical components, see an appendix.

5.3.2.1 Stepper motor controller

The positions of the translation stages are controlled by a Klinger CC-1 programmable stepper motor controller. The CC-1 drives the stepper motors of the stages in response to commands entered from the front panel or from computer control. Stage position was controlled from the front panel during alignment and focussing procedures, and from the IBM PC by way of an IEEE-488 port during testing. Stage translation velocity and acceleration are adjustable from either the front panel or from external control.

5.3.2.2 Bragg cell driver

The Bragg cell driver drives the electrical signal that causes Bragg diffraction in the modulator crystal. Diffraction occurs in response to a control signal initiated by the variable delay timer. This signal varies from 0 to 1 volt, with 1 volt corresponding to maximum diffraction. The maximum power driven (and thus the maximum laser intensity pulsed) may be adjusted by a level adjust knob, however the level was never lowered below the maximum during the experiments in order to maximize the contrast ratio of the modulator.

5.3.2.3 IBM PC

An IBM PC was used to control the experiment. A serial port was used to communicate to the embedded controller, and an IEEE-488 port (from National Instruments) was used to communicate to the stepper motor controller. The PC was equipped with a hard disc drive in order to store test data and software.

5.3.2.4 Embedded controller

The embedded controller consists of an 80188 microprocessor working at 3.07 Mhz, 8K of RAM, 8K of ROM, and an RS 232 port. It is capable of serial data communication with an IBM PC, and controls the fixed and variable timers, as well as the interval timer. It collects data from the test bed electronics and transfers test and control data to and from the IBM PC.

5.3.2.5 Master clock

The master clock is a series resonant 50 Mhz crystal oscillator buffered by 74AS04 inverters in order to form the clock signal for the variable timer and the frequency synthesizer circuitry.

5.3.2.6 Variable delay timer

The variable delay timer consists of two one shots, with digital main counters and ramp circuits to improve registration. The first one shot determines when the laser pulse starts and the second one shot determines when it stops.

5.3.2.7 Frequency Generator

This circuit generates the clock signal for the DUT. The signal generated may vary from approximately 1.8 Mhz to 46 Mhz in one kHz increments. The generator accepts a control signal from the embedded controller which sets the frequency of operation. The circuit also aids in coordinating the laser timer to the DUT clock.

5.3.2.8 Vector generator and capture board

The test vector is stored in an eight kilobyte EPROM with a 100 ns access time. Output vector capture is accomplished by a two kilobyte by 24 bank of fast static RAM memory. This fast memory is arranged in a pipelined fashion in order to increase the possible capture rate. This fast capture rate was originally implemented in order establish the capability of implementing a physical capture of the voltages on the output pins of the DUT. The capture board configured in this configuration will work as a memory based logic analyzer. This physical capture routine, however, was not implemented in the final experimental test plan. A logical capture routine was used instead, where the DUT writes logical values the capture memory during the course of the experiment. The memory is scanned for logically incorrect data each time new values are expected in the capture memory, with incorrect data corresponding to a logic failure. In this memory configuration, only eight bits of the 24 available memory bits are used.

5.3.2.9 Sequencer

The sequencer is a state machine which coordinates the timing between the execution of the DUT test vector, the laser illumination, and the frequency generator. The sequencer is used only during the state rank test. It's purpose is to insure that the proper state is illuminated with each application of the test vector. In is necessary because a microprocessor will require different amounts of time to reset after the application of each reset signal.

5.3.2.10 Noise Filter

A filter was added to the original test electronics in order to reduce voltage noise in the Bragg cell driver control signal. The filter is electrically switched into or out of the Bragg cell driver intensity control line by a control signal initiated by the embedded controller. This filter is

active on the line during the node ranking test, and switched off of the line during the state ranking test. The filter's 3 dB cutoff point is 150 KHz.

5.4 Test Bed Characterization

Several significant test bed electronics performance characteristics were measured and are presented here. The performance characteristics for the node ranking test will be reviewed first. Characteristics for the state rank test will follow.

The principle performance characteristics for the node ranking test involve the quality of the signal generated by the frequency generator and the quality of the Bragg cell driver control signal. The frequency generator has an absolute accuracy of approximately 600hz. This is primarily because the master oscillator was not exactly a 50 Mhz crystal. The output noise bandwidth of the frequency generator was approximately 50 Hz. This value is a measure of the frequency repeatability of the frequency generator. The Bragg cell driver control signal was accurate to within 5 percent or less of its programmed value. The noise in this line was generated by the circuitry in the variable timer circuitry.

The power supply common mode noise into the chip was approximately .4 volts peak to peak. The read time of the fast memory was 35 ns. This corresponds to a 22 Mhz maximum clock rate for the DUT. Had the memory been used in the pipelined mode, the maximum speed of operation would have been twice the given frequency. The EPROM used to store the test vector had an access time of 100 ns.

The principle performance characteristics of the state rank tests involve the timing of the laser. The worst compensated delay aberration in the laser timing was approximately two ns. The maximum rise time of the pulse width was 7.0 ns, while the fall time was approximately 6.5 ns. Noise in the Bragg cell driver control signal was approximately 100 mv.

5.5 Test Procedures

5.5.1 OVERVIEW

The procedure evolved over a period of weeks as different techniques were used in order to improve the

quality of the results. The test plan shown below is the final form. Flow charts are provided to aid the study of the test procedures. The test procedure consists of several steps, each of which will be detailed below in a step by step fashion.

The DUT is first prepared for testing. The die to be examined is first exposed and placed in the electronic test bed. The die is next powered up and tested to insure proper operation in the test bed and to check for damage from the exposure process. The die is next leveled and aligned. It is now ready for testing.

Testing begins by finding the maximum frequency of operation for the DUT. The DUT clock is then set to 99% of the maximum operating frequency. The die then is positioned under the laser and illuminated. If the outputs of the DUT are flawed as a result of this illumination, it is assumed that the laser is illuminating a node, and node and state rank data is taken on that position. If the outputs of the DUT do not show an error, the laser is positioned over another point, and the process is repeated.

During the node ranking procedure, the clock is reduced in frequency many times. With each frequency reduction, the laser intensity necessary to cause a failure at the outputs of the DUT is determined. In this manner, the curve described in Section 2 can be experimentally obtained.

State ranking involves first illuminating the clock cycles of the test vector individually and checking for faulty outputs from the DUT. Those states which generate faulty outputs are assumed to have critical timing. States with critical timing are then illuminated again. On each state, the level of laser illumination necessary to cause faulty outputs from the DUT is determined. States with more critical timing will require less laser illumination to cause logic failures at the output of the DUT.

There are several steps in the procedure that require a binary search pattern. In a binary search, the object of the search (often frequency or laser intensity) is varied in successive tests in a manner that will bring the object of the test closer and closer

to a sought after threshold level. Whether or not the object of the test is raised or lowered in value is determined by the result of the basis of the test (often correct or incorrect DUT operation)

In a binary search, the object of the test is first brought to its median value and a test is made. If the basis for the test gives a positive result, the object of the test is raised by half the difference of the last known value of positive basis results and the last known value of negative basis results. If the basis gives a negative result, the object of the test is lowered by half the difference of the last known value of positive basis results and the last known value of negative basis results. In this way the value of the object gets closer and closer to its sought after threshold level with each iteration of the test.

The maximum value of the object is assumed to be a negative basis result, and the minimum value of the object is assumed to be a positive basis result for the purposes of the test. Each time a binomial search is used in the experimentation, seven iterations will be used or the test will be carried out to the accuracy of the equipment, whichever comes first.

During the course of these tests, the mechanism for determining the presence and magnitude of critical timing will be the illumination of the DUT by a laser in an attempt to force a logical failure at the output. It is possible that this procedure will cause the DUT to latch up. This is a situation to be avoided, as it can easily lead to a physical failure in the DUT. Each time that a faulty output of the DUT is detected, power to the DUT is shut off. It is then powered back up and the test vector is again input into the DUT with the frequency set to a low value. Improper operation indicates a latch-up has occurred and the chip has either failed temporarily or permanently. Permanent failure causes testing on the DUT to end. Temporary failure causes testing on the present point to end.

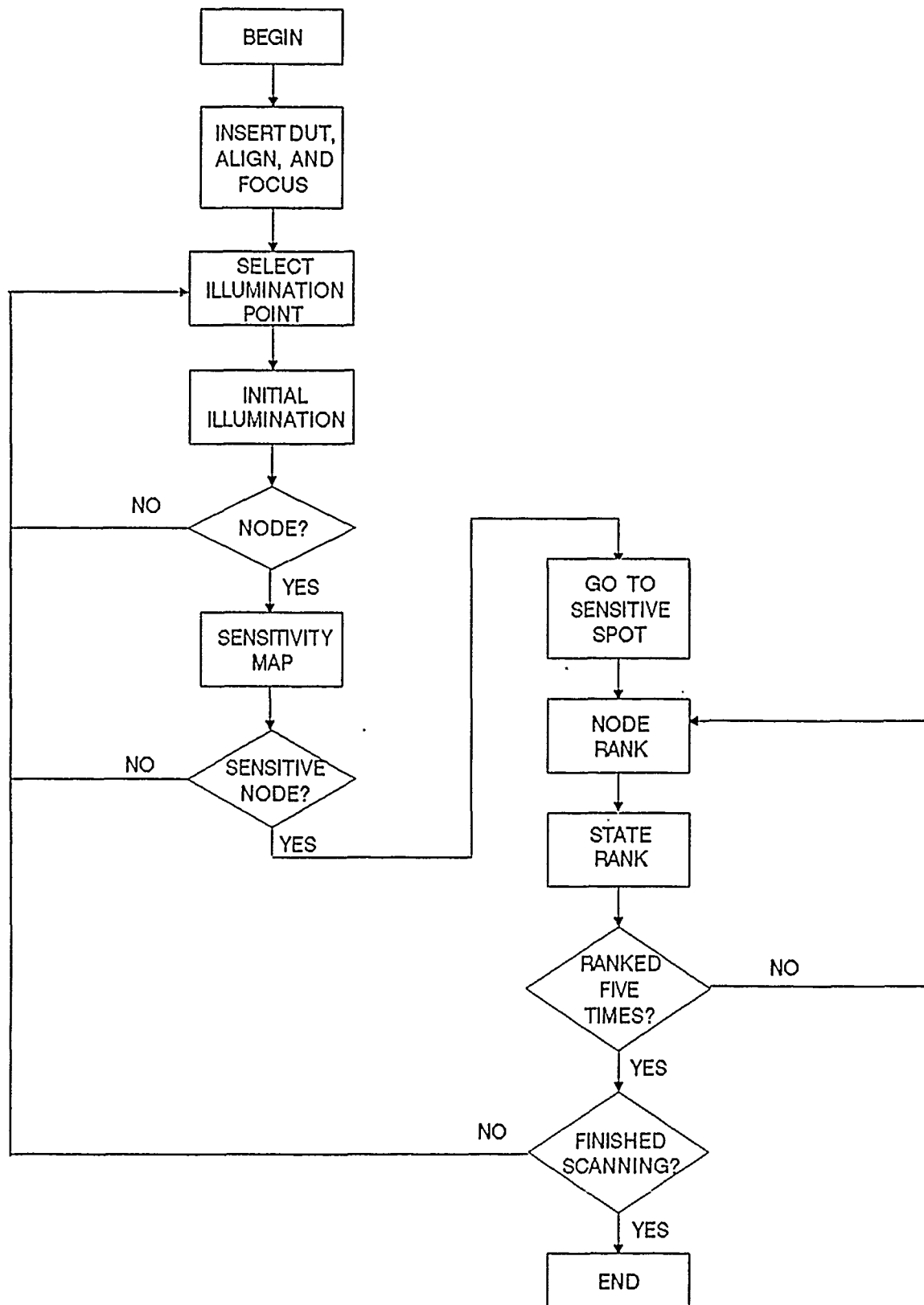


FIGURE 59: OVERVIEW FLOWCHART

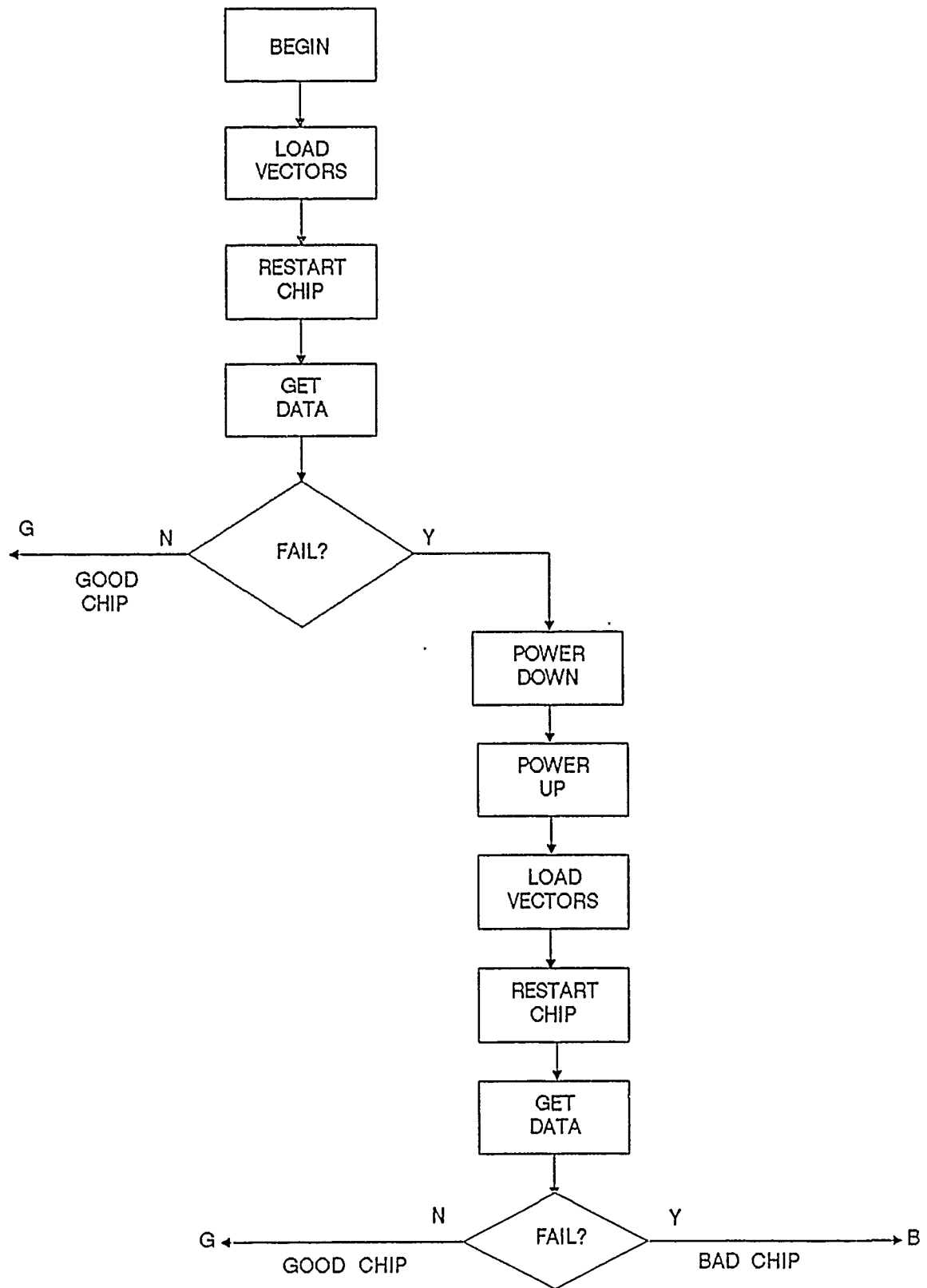


FIGURE 60: LATCHUP PREVENTION

5.5.2 Die Exposure

The first step of the experimentation is to expose the die in an already assembled package. This technique requires that the die to be exposed be in a ceramic dual in line package. A vise is prepared with a metal blades attached to both sides of the vice and arranged so that they faced one another. The Cerdip package is then placed in the vise with the pins facing up. Next the vise is closed with the blades on either side of the package and in the epoxy seam that separates the two ceramic halves of the package. Tightening the vice separates the two ceramic halves. Proper technique will insure that the die to package bonding will not be damaged.

5.5.3 Chip leveling

The exposed die is next placed into the electrical test bed. Care must be taken as the package pins are now delicately attached to the package by a thin layer of hermetic material. A zero insertion force socket in the test bed is required. The chip must now be leveled so as to remain focussed as the die is moved under the microscope. This is done by adjusting the tilt stage. Begin by adjusting the stage in two dimensions. Focus the microscope on a point on one side of the die. Next move the die in a manner parallel to the line between two of the three leveling screws on the tilt stage. Successive adjustment of the two leveling bolts will bring the die into focus in one dimension. Once the stage is leveled in one dimension, the other dimension can be brought into focus using the third leveling screw and by moving the stage in a direction perpendicular first set of movements.

5.5.4 Die alignment

Alignment is performed mathematically. In order to insure repeatability across several chips, it is necessary to define the stage position of two points on each die. In the experiment, mask fiducial marks found in each corner of the die were used. One fiducial mark was moved to stage position 0,0 (center stage.) The X-Y stage position of the second fiducial mark was then

determined and recorded. By knowing the relative stage positions of fiducial marks between two dies, an absolute position on each die may be located.

5.5.5 Find the highest frequency of operation

The highest frequency of operation of the DUT must first be determined under conditions of no illumination. A binary search will be used. The object of the search will be the frequency, and the basis of the search will be correct DUT operation, with a positive result corresponding to correct outputs and the negative result corresponding to incorrect outputs from the DUT.

5.5.6 DUT point of illumination selection

The limits of the active area of the DUT as defined by the stage travel must be determined. All points illuminated must fall within this limit. The points illuminated by the laser form a rectangular grid of a chosen number of rows and columns. The distance between the rows and columns is also chosen, as is the location of one corner of the grid. Once the grid is defined by the operator, the stage will move from point to point under computer control, examining each point in succession.

5.5.7 Valid node determination

The frequency is set to ninety-nine percent of maximum and the point in question is illuminated by the laser at 6.25 percent of maximum Bragg cell transmission intensity into the microscope. If no logical failure is detected at the output, the transmitted laser intensity is doubled and the point is examined again. This is repeated several times until the maximum possible transmitted laser illumination is applied to the point or the DUT gives incorrect output. If illuminating the point in question does not cause failure, the point is not a node with critical timing that we can effect with our laser, and it is ignored. If illumination does cause failure, the area around the point is scanned for maximum laser effect. The laser intensity entering into the Bragg cell is selected through the use of a polarizer to a value less than 2 milliwatts.

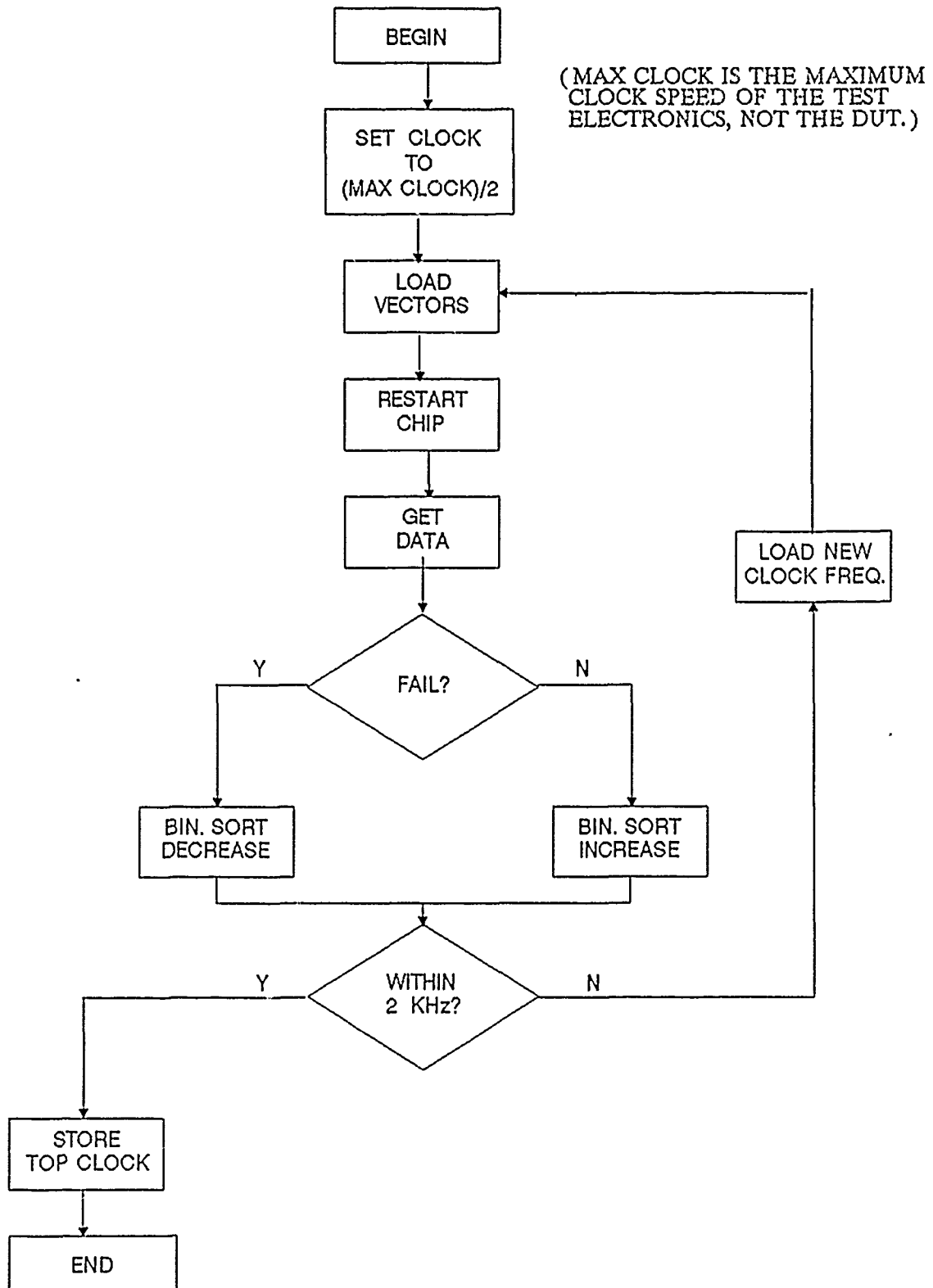
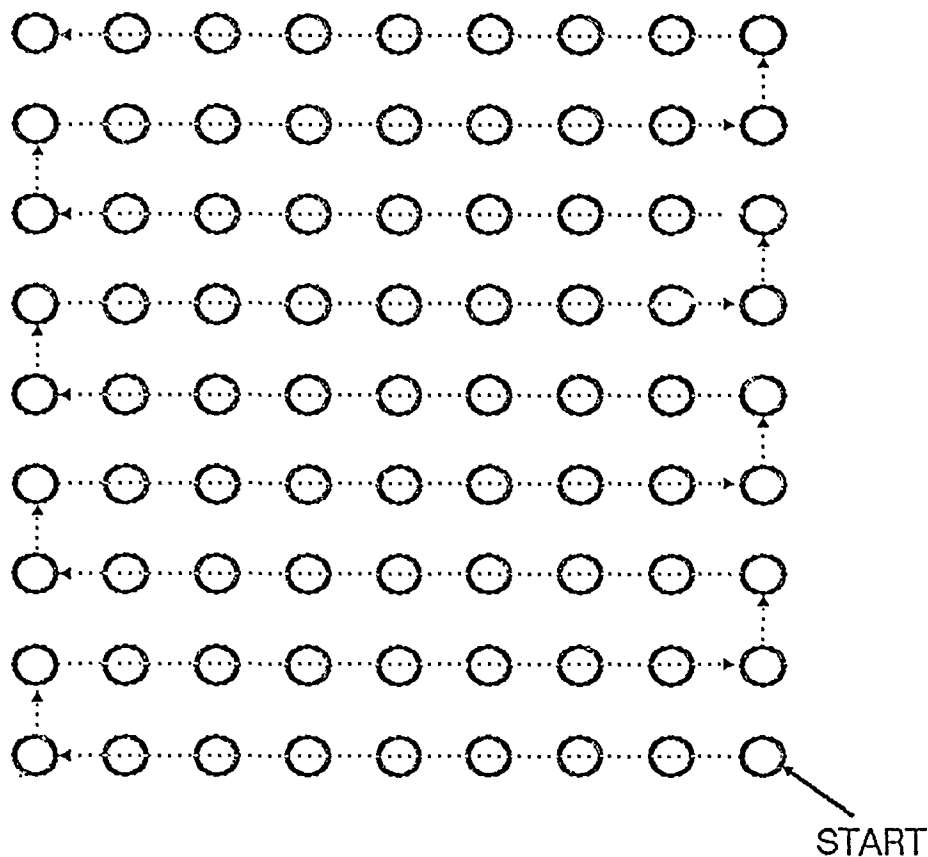


FIGURE 61: FIND MAX OPERATING FREQ.



PATTERN GEOMETRY DETERMINED
BY:

STARTING X COORDINATE

STARTING Y COORDINATE

NO. OF ROWS
AND COLUMNS

DISTANCE BETWEEN
ROWS AND
COLUMNS

FIGURE 62: LASER SEARCH PATTERN

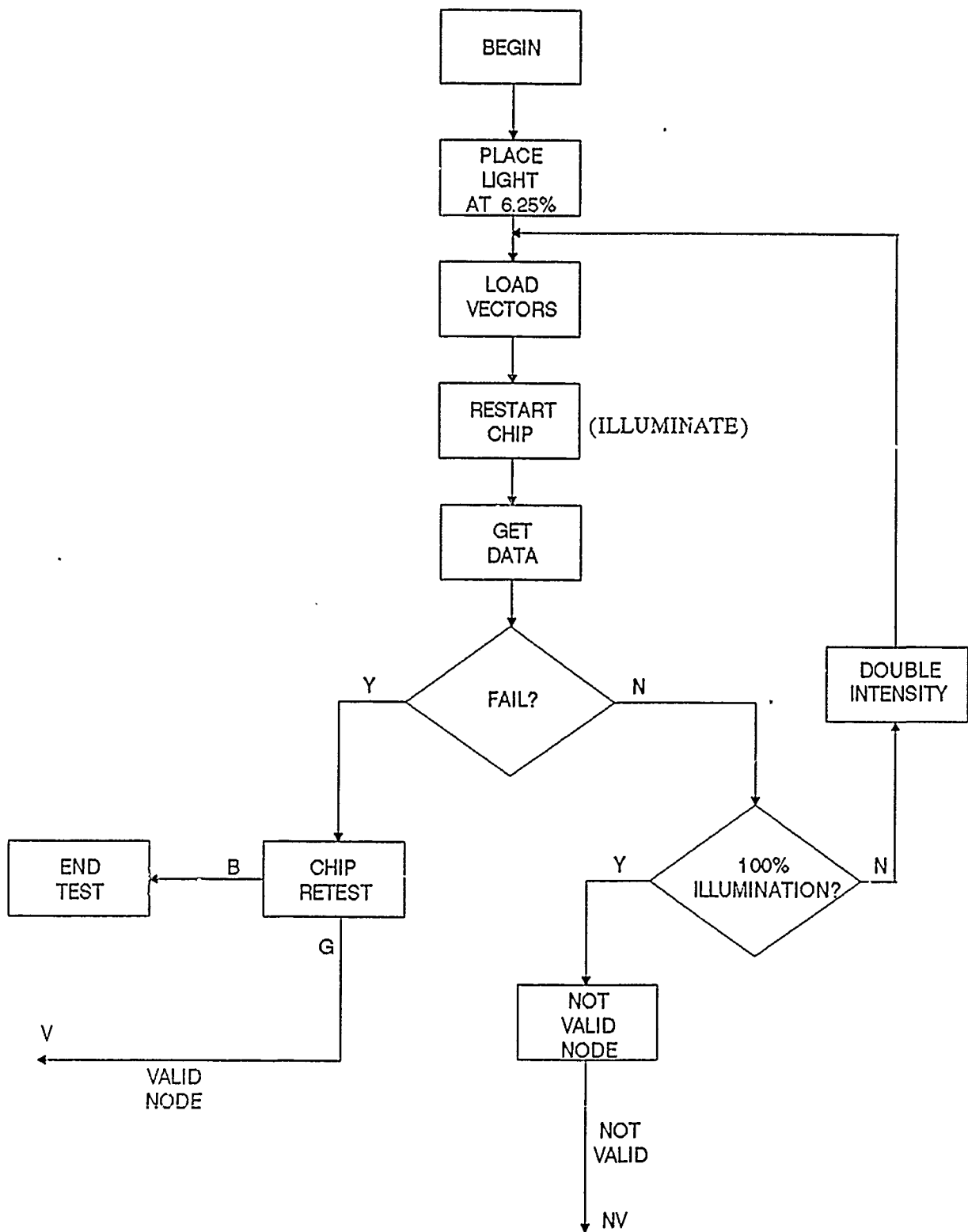


FIGURE 63: VALID NODE DETERMINATION

5.5.8 Laser effect scanning

Should an illuminated point reveal critical timing, the area immediately around the point is scanned. The purpose of the scan is to determine whether or not the laser will have sufficient effect on the node to warrant testing, and to determine the point where the laser has maximum illumination effect. The area of the scan takes the form of a square, with the original point in the center of the square. Step size of the scan is 1.5 microns, and the area is 115.25 square microns. Each point of the scan is tested using the valid node determination test. The point that requires the least laser intensity to cause failure is identified (this is the point of maximum laser effect). If this point requires more than 50 percent of the laser beam intensity to cause failure, then this node is not tested. If the point requires 50 percent or less of the maximum laser intensity to cause failure, then the point is node and state ranked.

5.5.9 Node ranking

This test is designed to determine the relative timing margin of one node with respect to other nodes in the system. This data is to be collected using the following procedure.

First, using the procedure above, find the maximum frequency of operation of the DUT five times. Select the average of these five values as the maximum frequency. One input into to test software is the number of points above maximum frequency that testing will start at. Multiply this number by 0.01 percent of the maximum frequency and add the sum to the maximum frequency to find the frequency at which testing starts. Set the function DUT frequency to this value.

Conduct a binary search with laser intensity as the object of the search and correct DUT operation as the basis of the search. The initial value of the laser intensity is to be the intensity that caused output failure found in the laser effect scanning 1. Line above rather than the median value. The basis of the search is to be the DUT output, with a logically correct output corresponding to a positive result. The laser is to

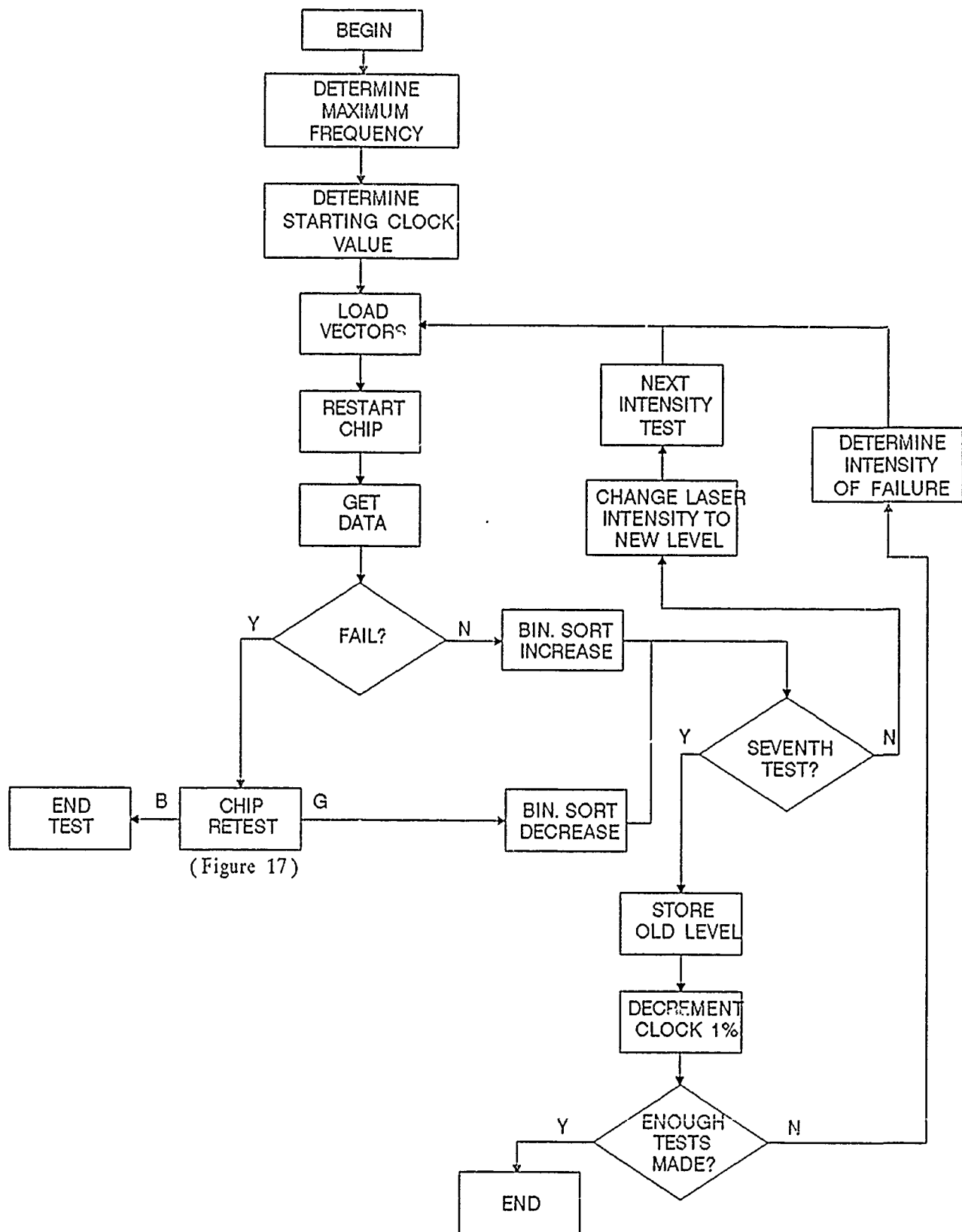


FIGURE 64: NODE RANKING PROCEDURE

continuously illuminate the DUT during each iteration of the test. Record the final laser intensity.

Next repeat the above binary search 129 times for a total of 130 tests. Each time reduce the frequency of operation by 0.01 percent of the maximum frequency of operation.

5.5.10 Recheck maximum frequency

Using the maximum frequency test detailed above, find the maximum frequency five times in succession. Select the average of these value to be the maximum frequency. Set the frequency of the DUT to forty kilohertz below the maximum frequency.

5.5.11 State ranking test

The state ranking test is designed to determine which states of the DUT have a critical timing associated with them, and of those states, which states have the most critical timing. To do this, the DUT is exercised with the given input vector many times, but with only one clock cycle illuminated by the laser each time. The test starts on the fourth clock cycle, and each clock cycle is illuminated in succession until the last clock cycle is illuminated. States that have a critical timing associated with them can be identified by logic errors at the output of the DUT. Once all of the states with critical timing have been identified, they are ranked by determining the amount of laser illumination necessary to cause logic errors at the output. This is a binary search with laser intensity as the object and DUT operation as the basis, with correct outputs corresponding to a positive result.

If during the course of the state ranking procedure a latch-up occurs, the laser intensity will be decreased by twenty-five percent. Testing will resume at the state in which the latch-up occurred.

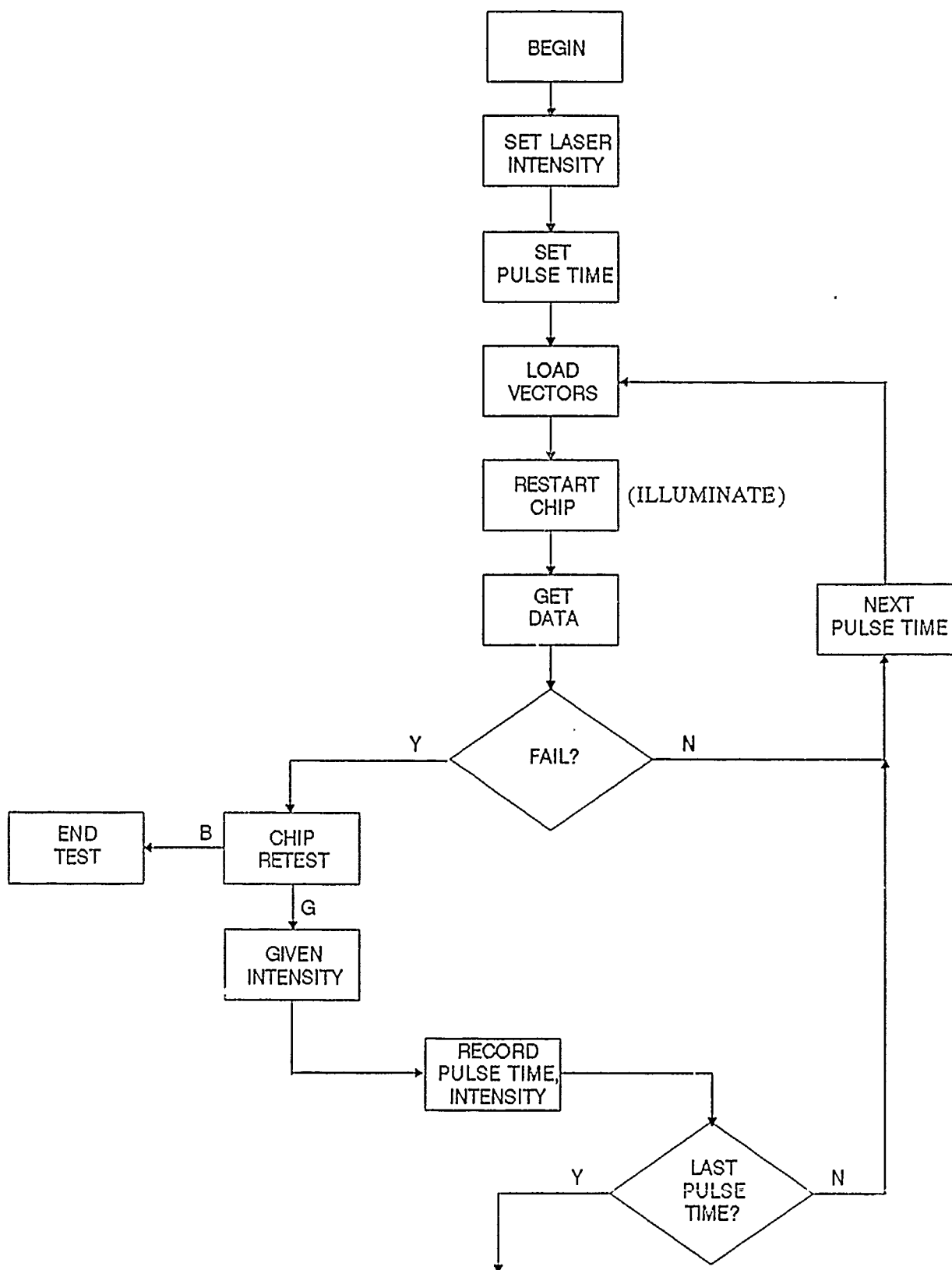


FIGURE 65: STATE RANK PROCEDURE,
PART ONE.

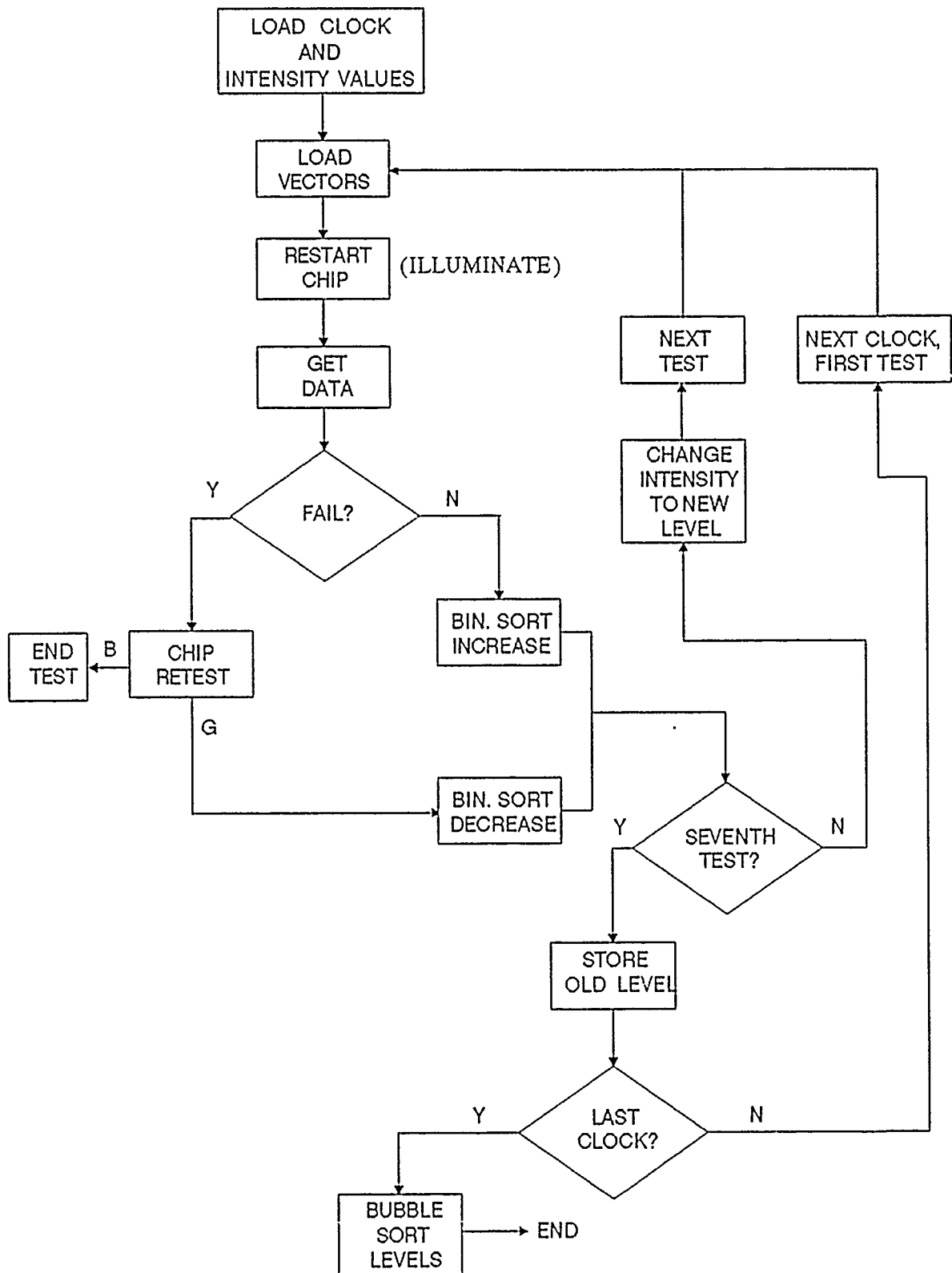


FIGURE 66: STATE RANK PROCEDURE, PART TWO

5.5.12 Repeatability test

This test is made to insure that the data that was collected in the above test can be collected again. Once a node has been node and state ranked, these tests are repeated on the node four more times.

5.6 Complex Test Data

A Harris 80C88 microprocessor was tested using the procedures described in Section 5.5. The test identified thirty-three nodes with timing margin. Of these nodes, three were found to have critical timing. States with critical timing were also identified.

5.6.1 Node Ranking Data

This section will present the data taken on three nodes during the course of the experimentation. Appendix three presents a complete listing of the node ranking data.

The data in this section is presented in the same manner as the Monte Carlo simulation data shown above. The three curves shown for each node ranking test give the actual data, the smoothed curve obtained from the regression technique, and the curve of noise magnitude.

The statistics and indicators show the noise and curve criticality indicators for each node ranking test, as well as the overall criticality indicator, and the regression statistics. The overall criticality indicator is consulted to determine whether or not a node is critical, with a value of one indicating criticality.

Test 7-28, Node 11

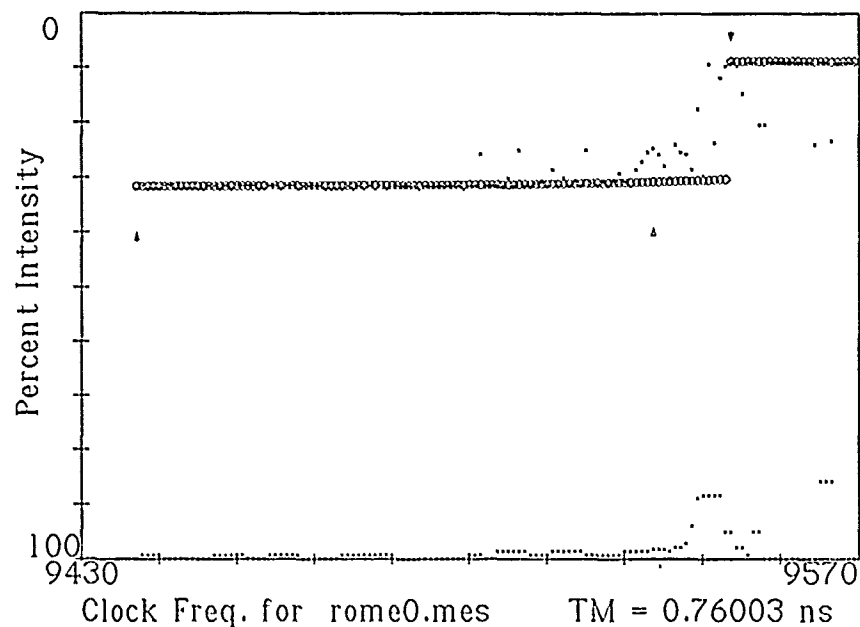


Figure 67: First node ranking of Node 11 of the test run begun July 28, 1989.

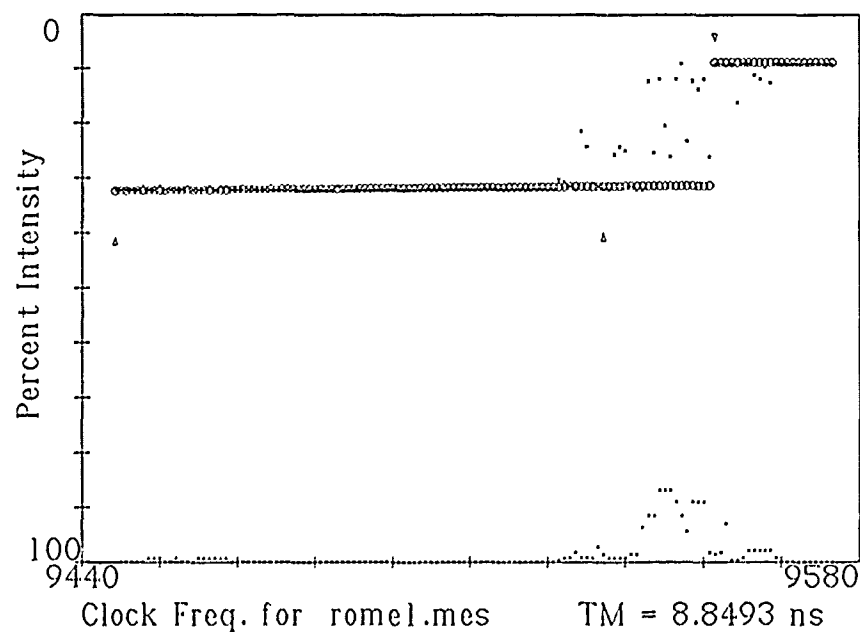


Figure 68: Second node ranking of Node 11 of the test run begun July 28, 1989.

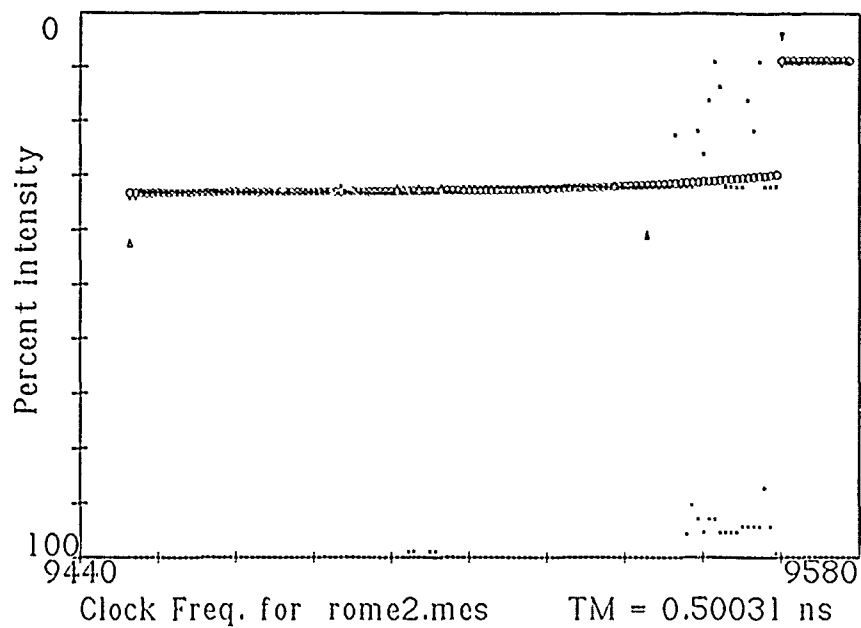


Figure 69: Third node ranking of Node 1 of the test run begun July 28, 1989.

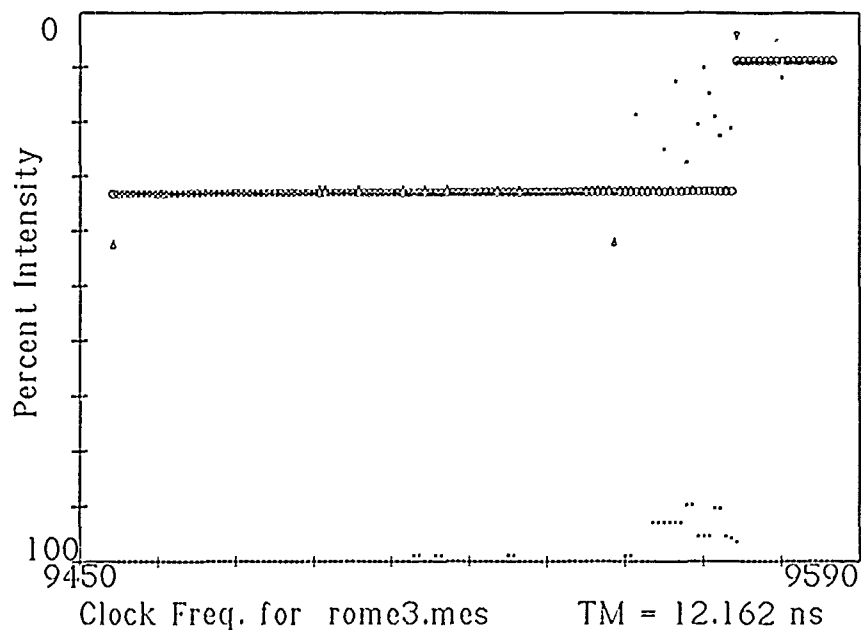


Figure 70: Fourth node ranking of Node 1 of the test run begun July 28, 1989.

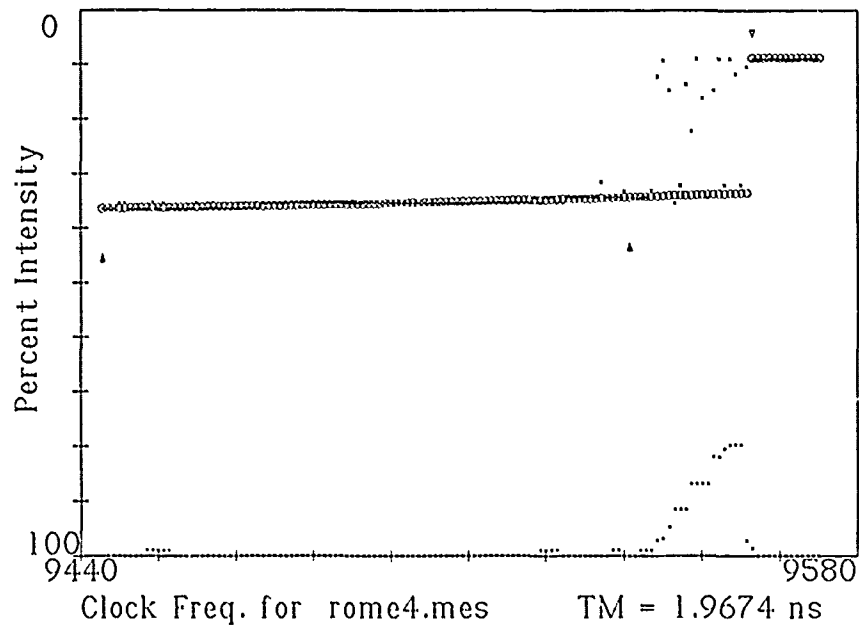


Figure 71: Fifth node ranking of Node 11 of the test run begun July 28, 1989.

TABLE 7

NODE STATISTICS AND CRITICALITY INDICATOR DATA FOR
 NODE 11 OF THE TEST RUN BEGUN JULY 28, 1989. THIS NODE
 WAS DETERMINED TO HAVE CRITICAL TIMING.

CN 0 = 1	CC 0 = 1	
CN 1 = 1	CC 1 = 1	
CN 2 = 1	CC 2 = 0	
CN 3 = 1	CC 3 = 0	
CN 4 = 1	CC 4 = 1	
C=1		
M=1.967413	A5=4.847722	S5=4.762568
A3=3.858919		S3=3.563005

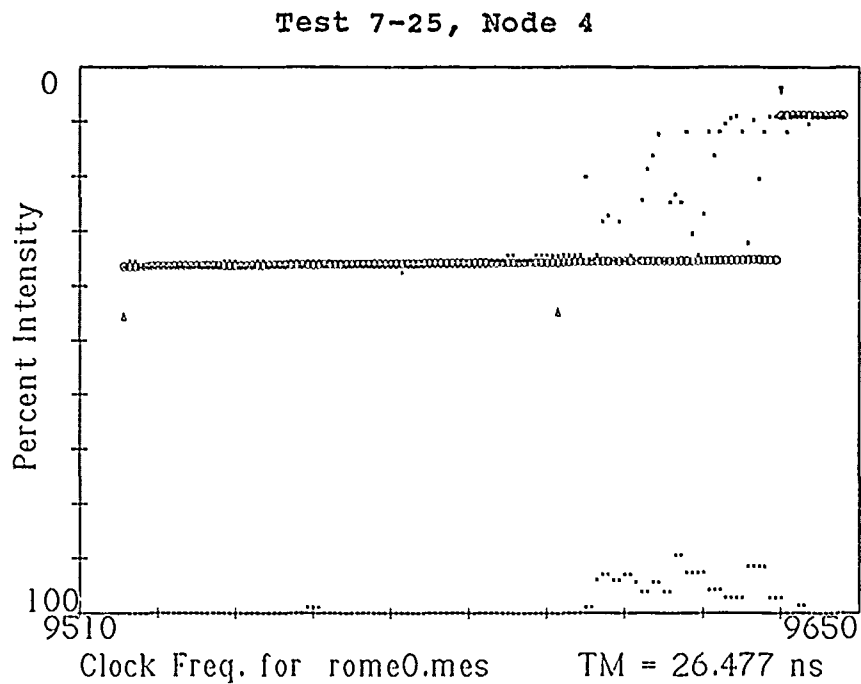


Figure 72: First node ranking of Node 4 of the test run begun July 25, 1989.

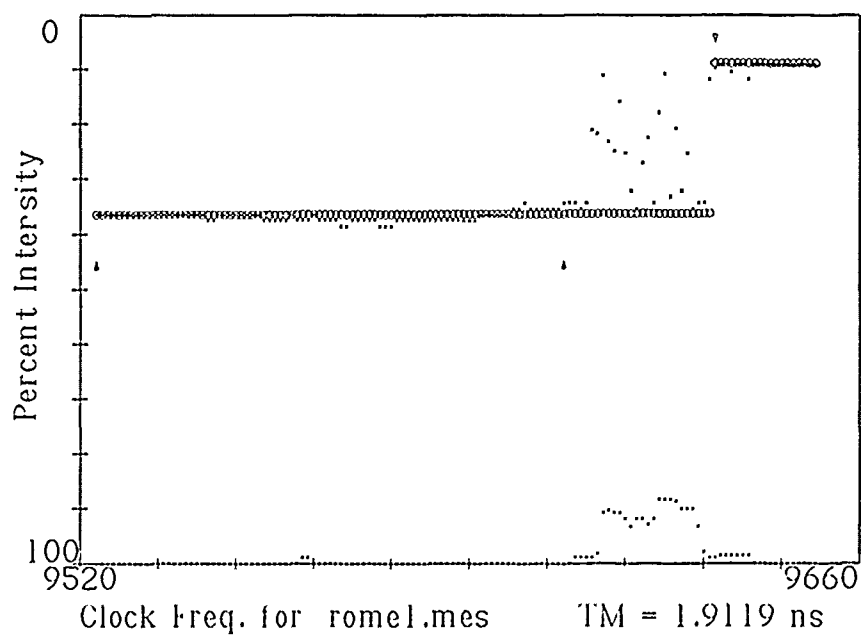


Figure 73: Second node ranking of Node 4 of the test run begun July 25, 1989.

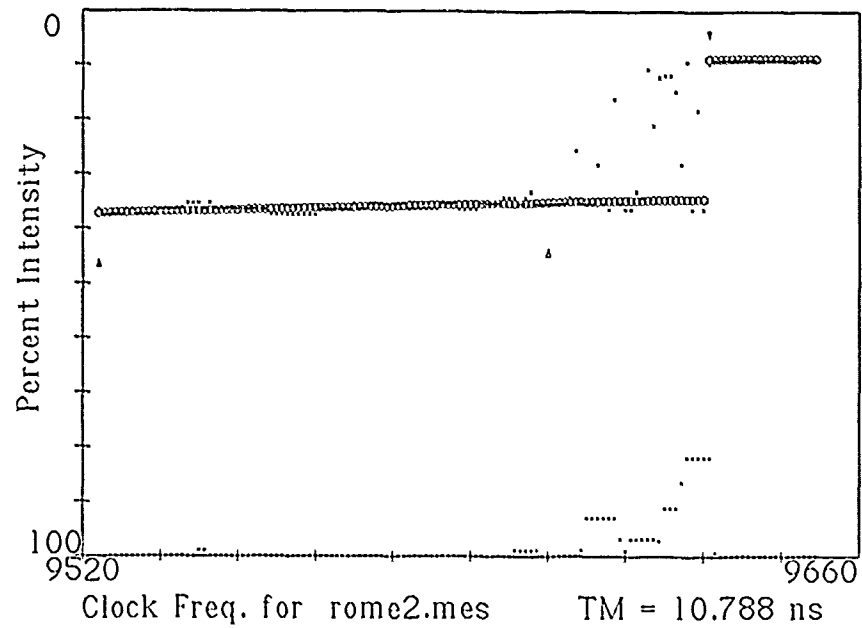


Figure 74: Third node ranking of Node 4 of the test run begun July 25, 1989.

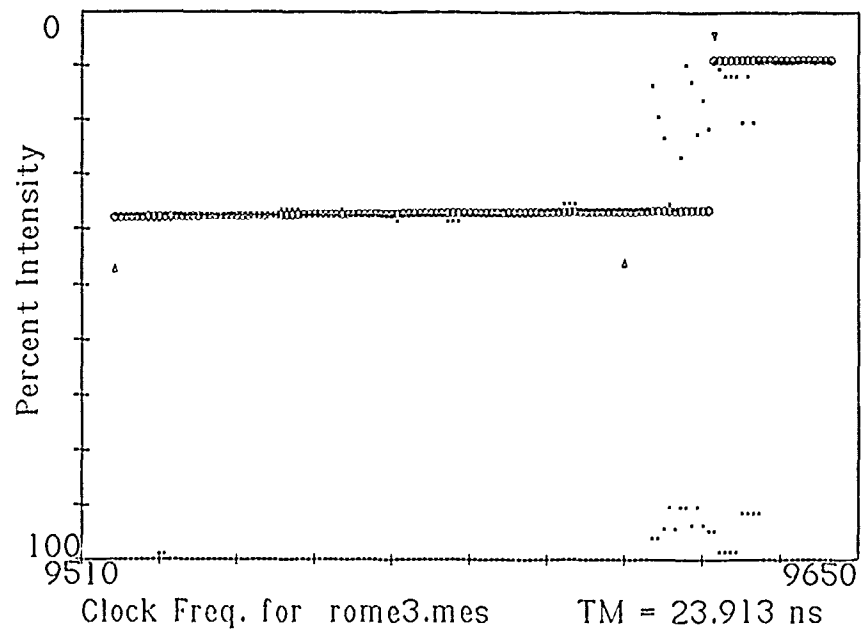


Figure 75: Fourth node ranking of Node 4 of the test run begun July 25, 1989.

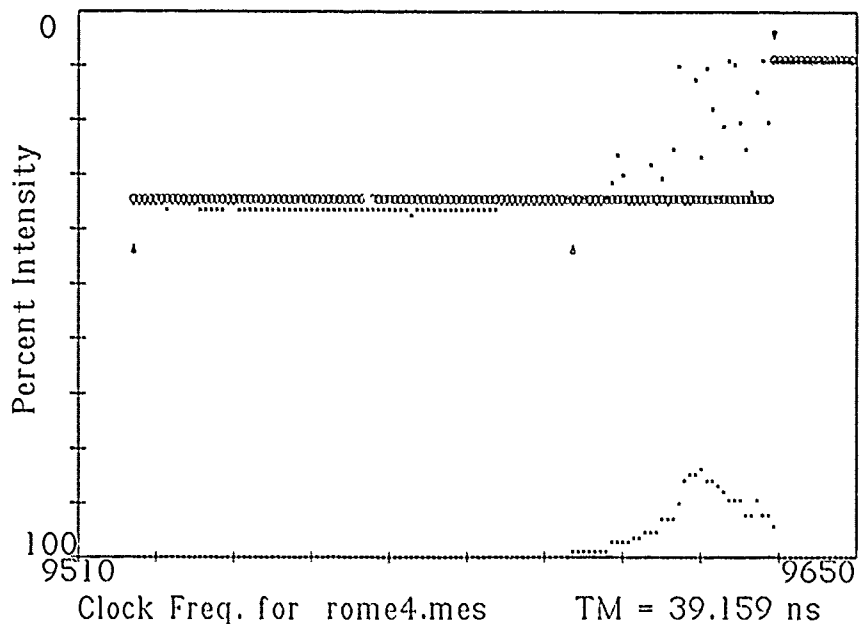


Figure 76: Fifth node ranking of Node 4 of the test run begun July 25, 1989.

TABLE 8

NODE STATISTICS AND CRITICALITY INDICATOR DATA FOR
 NODE 4 OF THE TEST RUN BEGUN JULY 25, 1989. THIS NODE
 WAS DETERMINED NOT TO HAVE CRITICAL TIMING.

CN 0 = 1	CC 0 = 1	
CN 1 = 1	CC 1 = 0	
CN 2 = 1	CC 2 = 1	
CN 3 = 1	CC 3 = 0	
CN 4 = 1	CC 4 = 0	
C=0		
M=23.91285	A5=20.4498	S5=12.92582
A3=20.39259		S3=6.872043

Test 7-28, Node 5

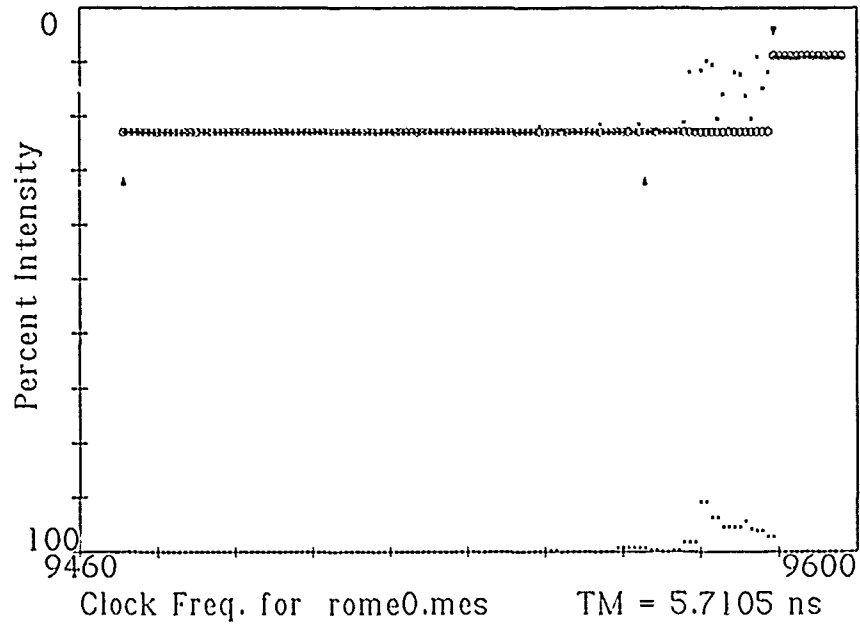


Figure 77: First node ranking of Node 5 of the test run begun July 28, 1989.

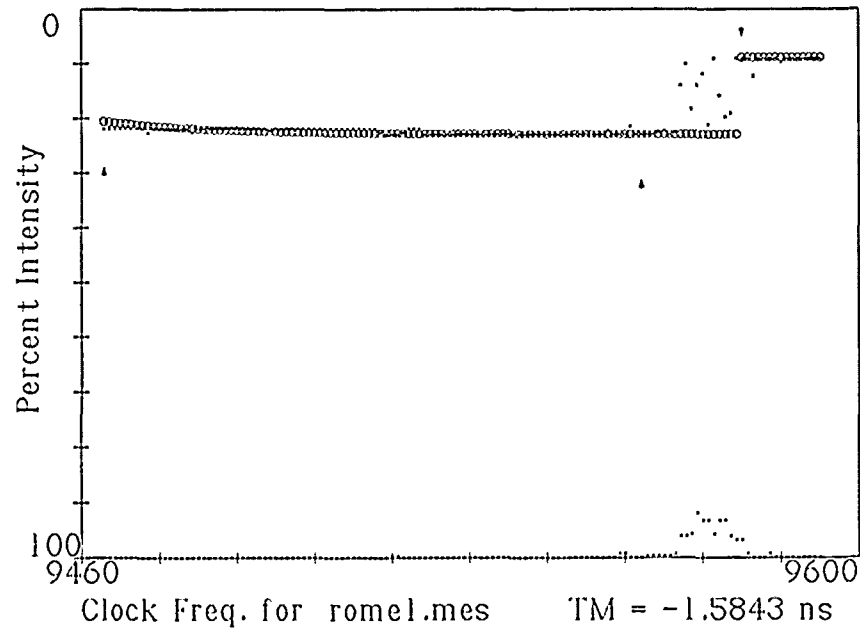


Figure 78: Second node ranking of Node 5 of the test run begun July 28, 1989.

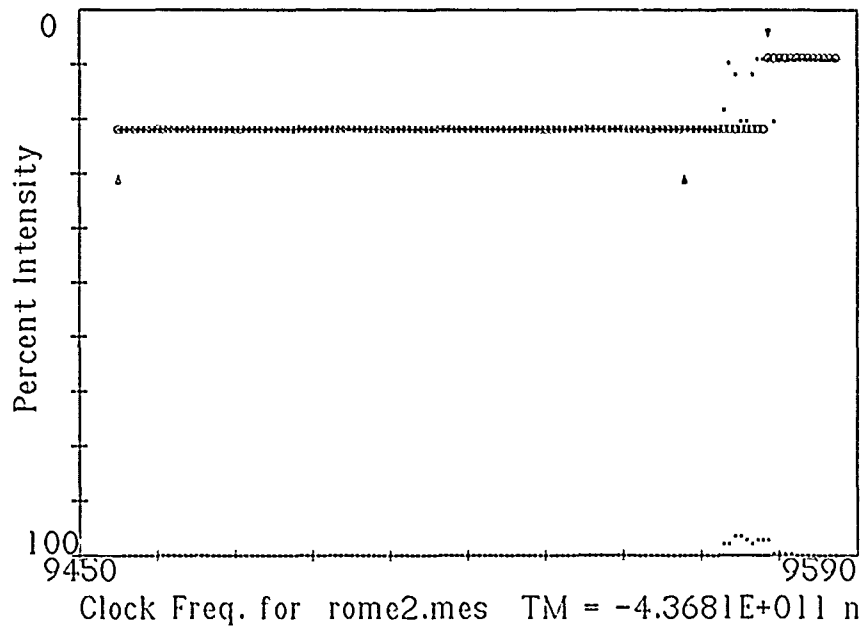


Figure 79: Third node ranking of Node 5 of the test run begun July 28, 1989.

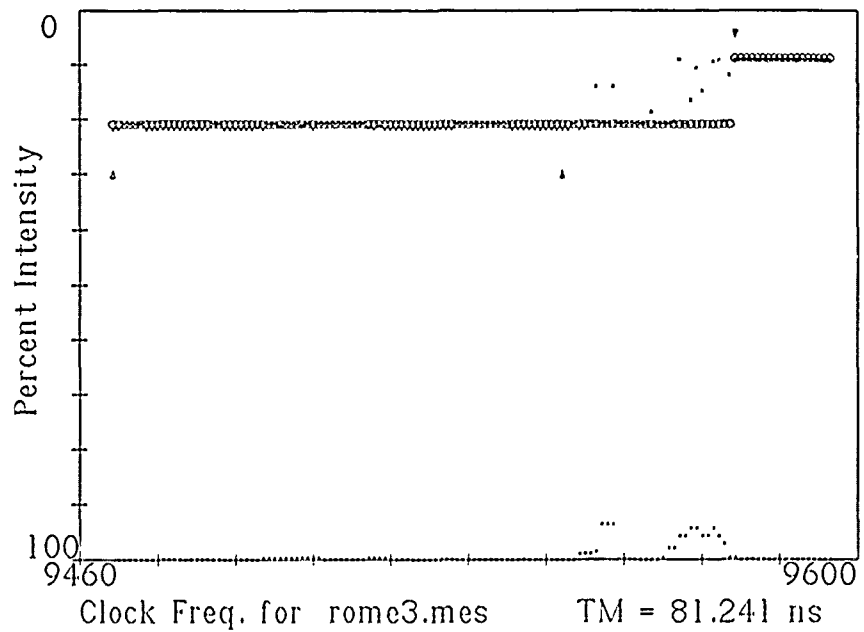


Figure 80: Fourth node ranking of Node 5 of the test run begun July 28, 1989.

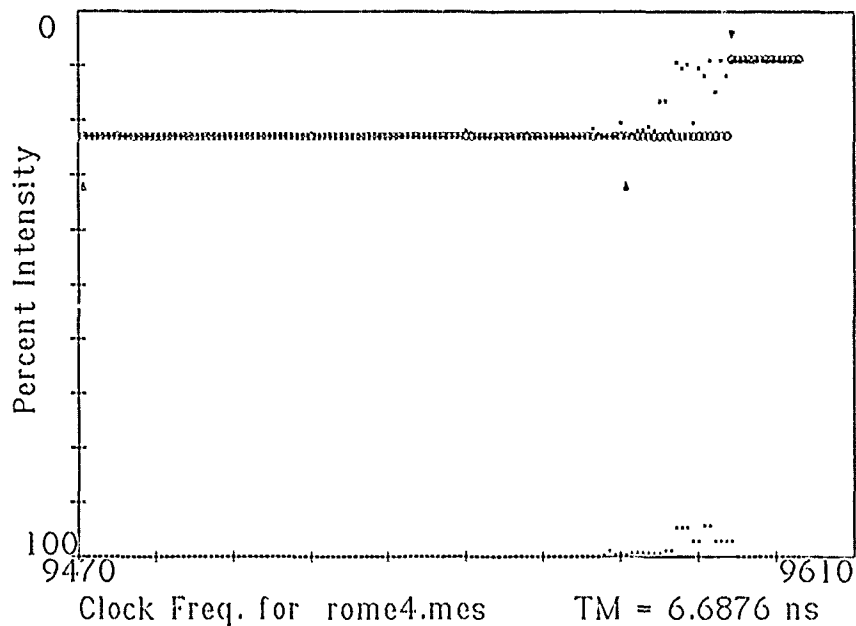


Figure 81: Fifth node ranking of Node 5 of the test run begun July 28, 1989.

TABLE 9

NODE STATISTICS AND CRITICALITY INDICATOR DATA FOR NODE 5 OF THE TEST RUN BEGUN JULY 28, 1989. THIS NODE WAS DETERMINED NOT TO HAVE CRITICAL TIMING.

CN 0 = 1	CC 0 = 0
CN 1 = 1	CC 1 = 0
CN 2 = 1	CC 2 = 0
CN 3 = 1	CC 3 = 0
CN 4 = 1	CC 4 = 0
C=0	
M=5.710527	A5=-8.736e+010 S5=1.7472e+011
A3=3.604615	S3=3.690723

5.6.2 State Ranking Data

The state rank data indicates that states that have critical timing may be spotted using this technique. Certain states were identified repeatedly at certain nodes. At other nodes, critical states are poorly identified. The technique is therefore capable of identifying critical states. To this extent, the technique works and the concept has been proven. However, the frequency variant noise present in the data makes state identification difficult and time consuming. Complete state identification should be possible by applying statistical techniques to repeated state rank testing data.

The representative data shown below is presented in tabular form, with the state rank data from each of the five state ranks presented in five different column pairs. In each column pair, the first column displays the states detected in each test listed in order of most to least critical, and the second column contains the laser illumination intensity necessary to just cause a logic failure at that state. A complete presentation of the state rank data is presented in Appendix IV.

The data from each tested node is identified by test run and number. Each of the test runs are identified by the date in which they were begun. Data taken during a test run begun on July 25 will be labeled as a node found during the run of July 25 even if it was actually identified and tested on some later date. The node number indicates the order in which the node was found and tested during a particular test run. The five tests of each node are numbered consecutively from Test 0 to Test 4.

TABLE 10
CRITICAL STATE DATA FOR NODE 9 OF THE TEST RUN BEGUN
JULY 25, 1989.

TEST 0		TEST 1		TEST 2		TEST 3		TEST 4	
STA	INT	STA	INT	STA	INT	STA	INT	STA	INT
99	1.20	101	1.20	113	1.92	103	1.20	99	1.20
101	1.20	103	1.20			115	1.20	101	1.20
103	1.20	99	1.36			101	1.98	103	1.20
115	1.20							156	1.20
164	1.20							227	1.20
219	1.20							95	1.98
97	1.92								

TABLE 11
CRITICAL STATE DATA FOR NODE 3 OF THE TEST RUN BEGUN
JULY 28, 1989.

TEST 0		TEST 1		TEST 2		TEST 3		TEST 4	
STA	INT	STA	INT	STA	INT	STA	INT	STA	INT
97	1.08	97	0.80	97	0.83	97	0.83	97	0.77
99	1.15	99	0.86	99	0.92	99	0.89	99	0.83
188	1.18	101	1.06	95	1.14	95	1.08	95	1.02
212	1.19	95	1.11	98	1.20	101	1.15	101	1.12
101	1.20	96	1.20	101	1.20	96	1.20	96	1.20
111	1.20	98	1.20			98	1.20	98	1.20
118	1.20								
174	1.20								
181	1.20								
197	1.20								
204	1.20								
215	1.20								
225	1.20								
228	1.20								

Two sources of noise are apparently responsible for the partial list of states obtained by the state ranking technique. The first reason lies in the noise present in the test electronics during the state rank tests. This noise manifests itself as a variation in the voltage that controls the intensity of the laser during

the state rank tests. This noise has a small effect when high intensity pulses are needed. However, it has a large effect when low intensity pulses are needed. Because low intensity pulses are necessary to spot the states with the most critical timing, the test fixture noise has its greatest effect on states that are of the greatest interest to us. The noise may cause a state to be missed entirely during our test runs.

The second reason lies in the noise present in the maximum frequency of the DUT. In order to cause a timing failure, the laser must induce a propagation delay in the state of interest that is larger than the timing margin. Thus, states whose timing margin is larger than the longest possible induced delay cannot be measured or detected with this system.

Because of this timing margin constraint, it is necessary to set the frequency of test for the state rank experiments as close as possible to the maximum operating frequency of the DUT. The random variation in the maximum frequency makes this test difficult. If by chance, the test frequency is set too far from the maximum frequency of operation, fewer logic states will be detected. This results from an unacceptably large timing margin. If the test frequency is set to near the maximum frequency of operation, random variation in the maximum frequency will cause some states to appear to have critical timing, when in fact they do not.

5.6.3 Deviant Results

This section will present representative samples of data that do not conform to the expected exponential curve shape. There are four readily identifiable deviant data configurations which may be organized into two different causal categories. The first category contains data whose deviant shape is the result of improper test parameters, and includes the "out of window" configuration, and the "railed laser intensities" configuration. The "out of window" configuration results when the maximum frequency of operation is outside of the range of frequencies which are sampled with laser illumination. One cause of this occurs as a result of a maximum frequency variation

during the start of a node ranking which pushes the frequencies of test outside of the window of test. This problem was eliminated when the average of five frequency samples was used to determine the maximum frequency of operation at the start of each node ranking and state ranking test. The second cause occurs when the operators improperly initiate the test.

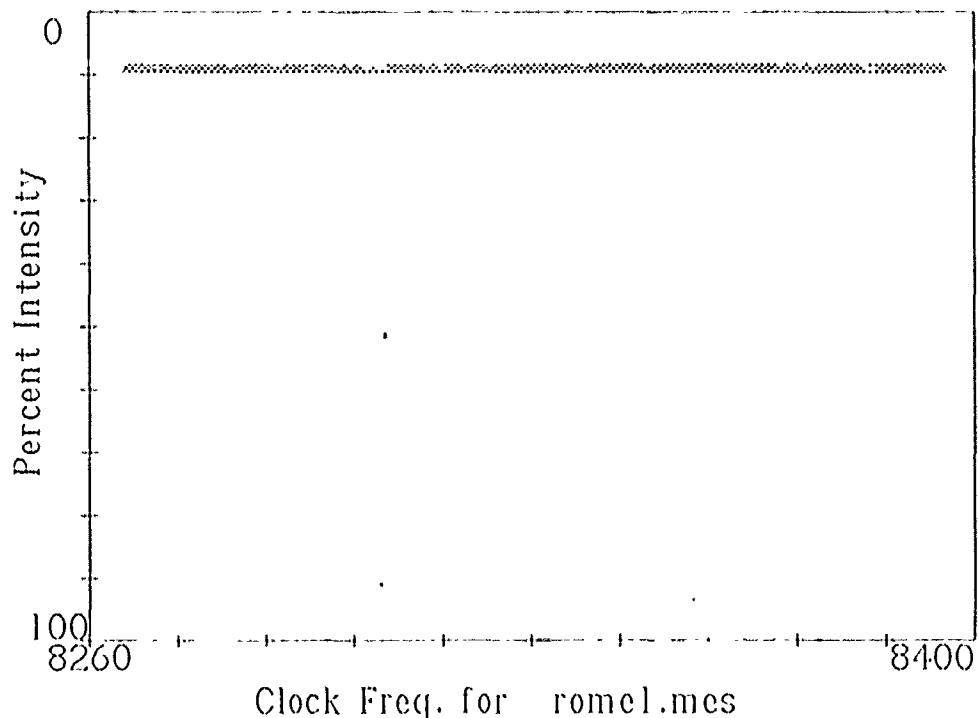


Figure 82: Deviant Data, "out of window" error.

The deviant configuration called "railed laser intensities" occurs when the node ranking test is applied to a node when the laser does not possess the necessary intensity to cause a logic error at that node. When this occurs, the data will appear as a straight line of maximum intensity. The data should not be interpreted as maximum laser intensity causing logic errors. It should be interpreted as maximum laser intensity having insufficient power to cause a logic error. This configuration of deviant results was eliminated by adding the scan for maximum effect routine into the test procedure. With this procedure, nodes which the laser is not capable of ranking are screened from the test.



Figure 83: Deviant Data, "railed laser intensities" for.

The second category of deviant results occurs as a result of unknown or unexplained phenomenon occurring at the semiconductor device physics level. The two common configurations are "negative slope" data and "highly variant" data. Negative slope data occurs as a definite and negative slope in the left hand side of the data, as shown in figure 84. This slope indicates that increased laser intensity is having a decreased effect on the timing margin of the node being tested. Clearly there is another mechanism effecting the propagation delay of the DUT at this node in addition to laser illumination. It is likely to be a first or second order phenomenon related to or caused by the laser illumination.

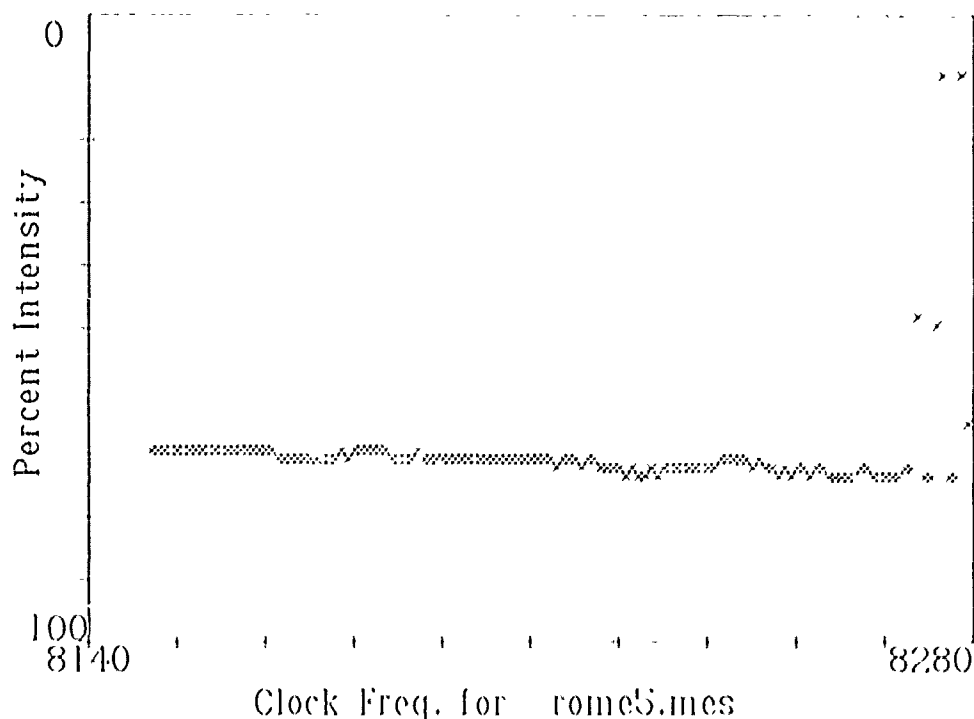


Figure 84: Deviant Data, "negative slope" data.

The deviant data configuration called "highly variant" data manifests itself in both positive and negative slopes as the shape of the curve takes on that of a somewhat sinusoidal oscillation to the left of the maximum frequency cut-off. An example of highly variant data is shown in figure 85. This form of deviant data may be related to the "negative slope" data. It is possible that both forms of deviant slope data result from heating effects at the DUT, or from the interaction of more than one node as the laser partially illuminates two or more nodes. Variant slope data is most often detected in first few nodes of each test run. This suggests that the cause is related to heating and transient effects. It is also possible that the ultimate cause of these data forms lies in some occasional spurious noise found in the Bragg cell driver electronics. Whatever the cause, for the time being this data must go unexplained.

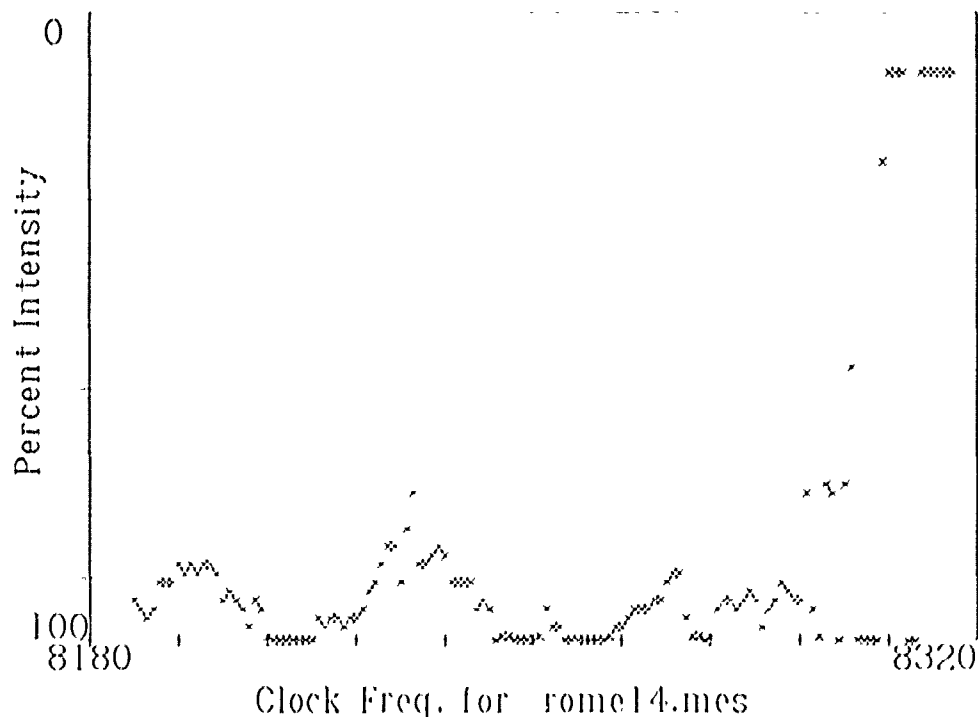


Figure 85: Deviant Data, "highly variant" data.

6 Conclusions

6.1 Simple Device Test Conclusions

It can be seen that Figure 30 can be compared to some of the results in the pulsed illumination test, especially the 2 volt p-channel cases. The test data has some interesting points in it, when the laser is attempting to increase the propagation delay.

a: The low voltage tests (2 volts) are more sensitive to illumination than the high voltage cases. The transistors do not have as much gate voltage and as such does not have as much drain current control. The illumination current does not change, however.

b: The greater the intensity, the greater the propagation delays affected.

c: The inverters with the propagation delay changes will have flattened (truncated) peaks for long laser pulse widths, as the delays introduced here will depend not on laser pulse width, but on intensity only.

d: The curves peak on the right for long propagation delays and laser pulse widths. This is only consistent

with the input pulse being active at that time. If the inverter propagation delay is small, and the laser pulse wide, the peaks will tend to be centered.

e: The test equipment is limited to test devices at 25 MHz and below. The laser pulse and inverter contribution at the shortest possible pulse width (10 ns) produces an effect 25 nanoseconds wide.

It can be shown, definitely, that this test does in fact test the propagation delay of an inverter under different situations.

The simplified model for inverter performance is generally accurate enough to characterize complex device behavior, when understanding the test data, although the model comes shy of true acceptance for describing theoretical behavior of a simple device. If this model is used only for empirical resolution of complex device data, and not a theoretical basis for performance, this model is adequate to describe in simple terms the inverter behavior. If a more complex understanding of inverter behavior is required for complex device analysis, the more rigorous theoretical forms can be used.

Device latchup, while not a problem in devices under normal operation, may be a problem when the device is being illuminated. This sets a degree of reason in which to base how nondestructive this contactless die probing technique really is. The author's suggestion is to either improve latchup protection on every device, or to restrict the testing to lot quantities selected from a main production run.

The propagation delay, as well as the output voltages and drain currents, and in extreme cases, logic outcome, can be altered using laser photoinjection characteristics. While voltages cannot be measured using this technique, the effects produced can relate to device operation by the effects on performance. The timing margin on a complex device, can be altered as well as the logic operation of a device, both are tools to check the operation and performance of a CMOS device.

6.2 Complex Device Test Conclusions

Over the course of the research effort, opportunities for improving the technique were discovered and several unexpected difficulties were encountered. The test plan itself evolved over a period of several months of discussion and planning. Even after the experimentation had begun, the test procedures underwent several major revisions. This chapter will review the advances and difficulties that were encountered during the research.

6.2.1 Improvements in Theory

The original test plan called for identification of individual nodes within a circuit, and then probing those nodes to determine the size of their capacitive loads and the transistor parameters of the gate at the node. Once these parameters were known, laser illumination could be used to alter the timing margin in a well understood fashion, with calibrated illumination levels yielding predictable propagation delays.

The original test designers understood that the effect of the laser was dependent upon the gate transistor parameters and load size. They believed that an industrial application was possible if a technology was well known and could be sufficiently modeled.

There were several disadvantages to this technique. First, the technique was technology dependent. One had to know the threshold voltages and other circuit parameters associated with each technology that was tested. Secondly, the technique assumed that there was no variation in the transistor parameters from one transistor to another within a technology. Third, the technique required a knowledge of the load capacitance associated with each gate. Much of these disadvantages could be overcome with a thorough knowledge of the production technology of the DUT, a good software modeling tool such as SPICE, and a knowledge of the DUT layout. The quality of the modeling would limit the accuracy of the technique.

There is another variable, however, that ultimately limits the accuracy of the original technique. The technique is heavily dependent upon the repeatability of the laser photocurrent injection process, however it is difficult to determine how much of the beam is being absorbed by the silicon in the space charge region surrounding the transistor drains. There are two phenomenon that limit the ability to model the photocurrent injection. The first involves the geometrical relationship between the beam and the transistor. If the laser is not positioned directly over the space charge region, but is instead off to one side or the other, a lesser amount of carrier generation will occur. Photon absorption might also vary with transistor geometry and doping.

Secondly, VLSI devices today consist of layers upon layers of thin films. Reflection and refraction effects the beam intensity at every thin film boundary. Also, the surface of a CMOS device is not smooth but broken. This is the result of several process steps that involve masking and etching. For this reason, the angle at which the laser beam strikes the surface and thin film boundaries is not constant. This further complicates the problem of determining the amount of photons that reach the depletion region and generate charge carriers. It is noted that both of these problems could be solved by measuring the supply current induced while the illuminated node is reverse biased.

For these reasons, a second technique was developed. This is the technique described in Chapter two. To summarize the technique, the timing margin at a node may be found by determining the laser intensities necessary to cause a logic failure at several different frequencies and then projecting the curve connecting these points back to the illumination equals zero axis. The new technique was developed in an attempt to eliminate the modeling dependencies of the original technique. Its major advantage is that it works independently of transistor parameters, gate output loads, and the ratio of beam intensity to charge carrier generation so long as this ratio remains constant during

the test. Experimentation has revealed that there are several limitations to this new technique. These limitations will be discussed below.

6.2.2 Analysis of Laser Intensities

Laser induced failure limited the laser intensities used in the experimentation. Initial illumination of the DUT was carried out with laser intensities on the order of .96 milliwatts. During the course of the testing, the maximum operating frequency of the DUT dropped tremendously. A device that would previously operate at better than nine megahertz would now operate only at less than two megahertz. Subsequent testing suggested that the laser was damaging the DUT, and lower illumination levels were used. Final illumination levels ranged from .48 milliwatts to .68 milliwatts. Even with these low illumination levels, a slow degradation of the maximum operating frequency of the DUT was seen.

Reducing the laser intensities reduced the number of nodes that we could characterize. A compromise was struck. The higher the laser intensity was, the more nodes could be characterized, but the shorter the life expectancy of the chip. By reducing the laser intensity, we were able to characterize many nodes on a chip without causing serious damage to the chip.

It is likely that the present illumination levels will reveal most of the minimum geometry nodes with critical timing. However, critical timing in nodes of larger geometry and nodes that are partially or completely obscured with metalization may not be identified and may not be characterized.

A technique has been used to screen nodes that are sensitive to laser illumination. Once a node is found, a scan routine is initiated that searches the immediate area of the die and locates the point of maximum laser affect on the gate. If more than half of the maximum possible laser intensity is necessary to effect the timing at the point of maximum laser effect, that node is not tested. In this way, nodes that we are

not capable of characterizing are not tested. This screening has also caused a noticeable reduction in the rate at which the maximum frequency of the DUT declines.

It is possible that laser induced failure occurs only (or mostly) when non-nodal points are undergoing illumination. An example of this would be photocurrent injection occurring at well boundaries. Well boundaries occur fairly often in a complex CMOS device, and exist under approximately half of the transistors. If well boundary illumination is causing latch-up, selection of a different frequency laser (one that has less penetration depth in silicon) might further reduce the occurrence of laser induced failure. Further, a knowledge of the device layout would eliminate the likelihood of illuminating a well boundary at the surface of the die (where laser intensities are at their highest.)

Others have shown that photoinjection is useful for debugging latch-up. Areas which are more sensitive to latch-up require less laser intensities to induce latch-up. It has been reported that maps of latch-up sensitivity may be generated using a laser and beam scanning mechanism.

6.2.3 Frequency Stability

A second effect has been noticed that increases the difficulty of testing. Notably, the maximum frequency of the DUT is not a constant, repeatable value as one would expect, but varies over a range of frequencies. There are three possible factors that may contribute to this frequency variation. Each is likely to contribute to the variation in some manner. These factors are short term heating and cooling, long term heating and cooling, and laser induced failure.

There is a continuous frequency variation detectable in the DUT. For a new, untested and unilluminated chip, this range is approximately half on one percent of the maximum operating frequency. It is theorized that this is the result of small and continuously changing temperature variations in the DUT. This small gradient could be the result of slight

changes in environmental temperature, differences in power dissipation in the DUT due to changing transistor conductances, or perhaps a combination of the two. This variation occurs irregardless of laser illumination, although laser illumination may contribute to the problem.

A second effect is seen as a trend over time. When the DUT is started cold and unilluminated, it's maximum operating frequency is at it's highest value. Over the course of a few minutes operation, the average maximum frequency will decrease slightly and then level out at some new and lower level. It is theorized that this is the result of an increased ambient DUT temperature caused by power dissipation in the DUT.

The third effect is also seen as a trend over time, and is related to the intensity of laser illumination used in the test. Over a period of hours or days, the maximum operating frequency of the DUT will decrease markedly. This is laser induced failure and is believed to be the result of laser induced latch-up. As the DUT maximum frequency crept downward due to laser induced failure, the frequency stability became worse.

The frequency variation problem does not appear to result from the test fixture. The test fixture was examined for frequency stability and correct operation. The stability of the clock generation circuitry has been monitored during the tests and has proven to be stable to within one hundred Hertz over the frequency range of testing.

The frequency variation had adverse affects on the test results. The short term frequency variation resulted in noisy data whose information content was difficult to extract. The long term frequency drift slowly moved the test "window" in frequency out of the region of interest.

Changes were made in the test procedures in order to deal with the frequency variations using simple statistics. Whenever a test is made to determine if a particular combination of frequency and intensity causes a logic failure, the test is repeated 101 times. If the

majority of the results show a logic failure, then the test result is assigned to be a logic failure, and if the majority show correct operation, then correct operation is assumed. A numerical method was employed to extract the expected curve from the data.

Also, the maximum frequency of operation under conditions of no illumination was updated on a regular basis, and all test frequencies are related to the maximum frequency with no illumination. Whenever this maximum frequency was found, the 101 point test described above was repeated five times and the new maximum frequency value was assigned to be the average value of these five tests. This kept the test "window" in frequency in the region of interest.

Finally, steps were taken to minimize the possibility of latch-up. The laser intensity of the test was reduced to the minimum possible level that still allowed the test to take place. Further, a scan and screen routine was initiated that determined the position of maximum laser effect on the DUT for each node. If this intensity level for maximum effect was greater than 50% of the maximum laser intensity used in the test, the node was not subjected to node and state ranking. This screening was found to reduce the effect of laser induced failure. The screening also eliminated another problem. Valuable test time was no longer wasted by nodes that could not be node ranked with the maximum selected laser intensity.

6.2.4 Test Fixture Play

The stage and the microscope behaved in a way that was not anticipated. Once the anomalous behavior was spotted, procedures were developed to account for it.

The stage did not prove to be repeatable. When experimentation began, the stage was repeatable to within a few tenths of a micron. However as time went by, the stage began to be less and less repeatable. Over a series of automated tests that lasts dozens of hours, the test may be off by as much as ten microns in

any given direction. This may be due to mechanical wear or some other cause that the experimenters are not aware of.

As a result of this loss in accuracy, the test plan was altered. Once a node was located, that node was completely tested using the node rank and state rank procedures. The node and state rank procedures are then repeated five times each. Further, nodes were not cross-examined from one chip to the next.

The focusing apparatus of the microscope also proved to have play in it. Adjusting the focus would move the focal point of the microscope not only perpendicular to the chip surface, but also parallel to it. This was a problem because the focal length for the laser was different than the focal length of white light.

To overcome this problem, the microscope focus and alignment was accomplished in two parts. First, the microscope would be focused so as to generate a minimum size laser spot. Second, white light would be directed into the microscope so that DUT features could be distinguished, and the DUT would be properly positioned beneath the microscope. This repositioning was carried out while the microscope was slightly unfocused for white light, so there was an intrinsic loss of accuracy in the repositioning. This inaccuracy, however, was less than one micron, and did not affect outcome of the experiment.

6.2.5 Curve Fitting

The frequency variation noise associated with the experimentation made the use of a numerical method necessary. Eventually, a linear regression and criticality indicator technique was settled on. This technique is described in Section 3.

6.2.6 Stage Movement

The selection of a point for testing was originally intended to be a completely random process. The boundaries of the active area of the DUT as defined by the stage travel would be entered into the computer as the limits of a Cartesian coordinate grid. A random

point in the X and Y coordinates would then be generated and would undergo illumination testing. This worked well, but the time required to move from point to point between tests averaged approximately two minutes. This was unacceptably long, as dozens of points needed to be tested to find one node.

In order to speed up testing, a grid like search pattern was devised. Test points were illuminated in a raster like fashion, with the test sweeping from one raster to the next and searching points along each raster for nodes. The number of rasters and number of points searched per raster was entered at the start of each test, as was the starting location of the test (the beginning of the first raster sweep.) The distance between points in each raster was set to twenty microns.

As a result of this change, the time between tests was reduced from an average of approximately two minutes to just a few seconds. This greatly increased the rate of testing. It also allowed testing to be concentrated on specific areas of the DUT, which allowed repeated testing of one area. This second ability was useful during troubleshooting.

6.2.7 Test Magnitude Escalation

The test as it was originally conceived required one test for proper logical operation per illumination intensity in a binary search and up to 21 different binary searches per node ranking. The final version of the test was much more complex. At final count, 101 tests per illumination intensity were made in each binary search, and 135 binary searches were made per node ranking. The number of tests for proper logical operation per node increased from the original 21 to the final 13635, in addition to the 1010 binary searches that occur at the beginning and end of node ranking to find the maximum frequency. A similar escalation occurred in the state rank test. Conservatively, 500 million tests for proper logical operation were made during the course of the experimentation.

6.2.8 Test Fixture Noise

Noise in the test fixture manifested itself as a variation in the voltage level delivered to the Bragg cell controller. This voltage in turn caused a variation in the intensity of the laser exiting the Bragg cell. A filter developed during the course of the experiment greatly reduced the noise present during the node rank tests, but did not appreciably reduce the noise present during the state rank tests.

The test fixture noise, in addition to the noise in the maximum frequency of the DUT, made accurate and repeatable sampling of state rank data difficult. In order to improve the accuracy and repeatability of the state rank test, the noise in the state ranking electronics would have to be reduced.

6.2.9 Industrial Feasibility

The theory predicts that this technique may be useful in an industrial environment as a way to measure the timing margins of nodes and as a way of spotting the states with critical timing in those nodes. In an industrial environment, this may be useful for evaluating circuit improvements which are intended to reduce propagation delays in a signal path and increase the

f_{MAX}

of a device. In practice, the maximum frequency variation noise should be reduced to approximately twenty-five percent of the present measured value in order to make this technique valid. Without this reduction in the maximum frequency noise, the large numbers of tests necessary to examine each node would greatly restrict the usefulness of the tests in an industrial environment.

An increased rate of testing would increase the industrial feasibility of this technique. Presently in the test procedure, the time required for the phase lock loop of the frequency generator to lock onto its programmed frequency consumes a great deal of overhead test time. The overhead time is necessary because the frequency generator must switch back and forth between

high and low frequencies. The high frequency is selected during the illumination tests, and a low frequency is set after logical errors in order to test for latch-up.

A test scheme that reduced the large frequency changes would reduce the time necessary for the phase lock loop to stabilize, and so greatly increase the rate of testing. A two oscillator system would meet this requirement. One oscillator would consist of the existing frequency generator, and be used for maximum frequency testing and illumination testing. The other oscillator would consist of a single frequency oscillator set to a low frequency, and be used for latch-up testing after logical failures in the DUT. Switching between these two oscillators at the appropriate time would reduce the time necessary for the phase locked loop to stabilize between frequency changes by an order of magnitude, and so would significantly increase the rate of testing.

Perhaps a better use for laser photocurrent injection is in test vector validation. It has been shown that lasers may be used to set the logic level of a transistor in a complex CMOS circuit. This phenomenon may be used to measure the quality of test vectors applied to complex CMOS devices. A 100 percent test vector will exercise all of the logic in a DUT in order to insure that the logic preforms the functions required from the DUT. By setting the logic level of a gate, the logic of the DUT is altered. A good test vector will spot this alteration, while a poor test vector might not. By setting the logic level of gates in a complex device and applying the test vector, the quality of the test vector may be examined.

A third use of photocurrent injection explored uses the laser to examine subsurface features in CMOS devices. There are electric fields found throughout the silicon on semiconductor devices. In space charge regions, these fields are large. In bulk semiconductors, these fields are small, but present. Further, these fields change as the logic of the DUT changes from state to state. The electric fields around

an inverter will be different when the p-channel transistor is conducting rather than the n-channel transistor. These fields may be probed through the use of a laser and a current meter.

The features of a CMOS device may be examined by illuminating them with a laser. Small electric fields will yield small increases in current measured at the supply contacts, while large fields will yield larger currents. As a result different components, when illuminated by a laser, may be detected and discriminated from one another by measuring the corresponding increase in current at the supply rail. For a given laser illumination, active p-channel transistors will yield one current increase, metal layers will yield another, bulk silicon will yield yet another, and so on.

Using this knowledge, an image may be formed that depicts the surface and subsurface components of the illuminated CMOS device. The technique requires a small laser spot and an X-Y stage or some other means of directing the beam across the surface of the device in a precise fashion, and an accurate current meter. By moving the laser from point to adjacent point across the surface of the DUT in a raster like fashion while at each point measuring the increase in current drawn at a constant level of laser illumination, a map of the device surface is formed. This map may be displayed on a computer by assigning color or shading values to different ranges of current, assigning pixel values to each stage coordinate, and displaying the color that corresponds to each pixel.

A fourth application of laser photocurrent injection might make real time logic level probing of a transistor in a complex CMOS device possible. By illuminating a transistor drain with a laser whose intensity has an alternating amplitude component, and detecting monitoring the supply current for current variations of the same frequency as the laser intensity variations, active logic states in the illuminated transistor may be spotted. Whenever the illuminated transistor is "off", the frequency variation in the supply current should be

detected, and whenever the transistor is "on" & conducting, the supply current frequency variation should not be detected. Real time detection of the frequency variation in the supply current would make real time logic examination possible.

Appendix VI

TEST EQUIPMENT THEORY OF OPERATION

This appendix goes in depth into the test bed electronics and custom instrumentation that operates the laser and tests the various simple and complex devices. Most of the circuitry, that did the test interface with the device under test, was either AS TTL logic or ECL type logic. The design paid attention to UHF wiring practices, although the project was done on ground plane perforated board stock. Printed circuit stock, either double sided or multilayer could have improved the performance of the circuitry.

The theory of operation consists of two major sections: the simple and complex device test setups. The circuitry within each are discussed, when needed. If the discussion gets technical within the simple device sections, one can skip to the complex device test plan to get an overview of the complex device electronics.

Simple Device Test Plan

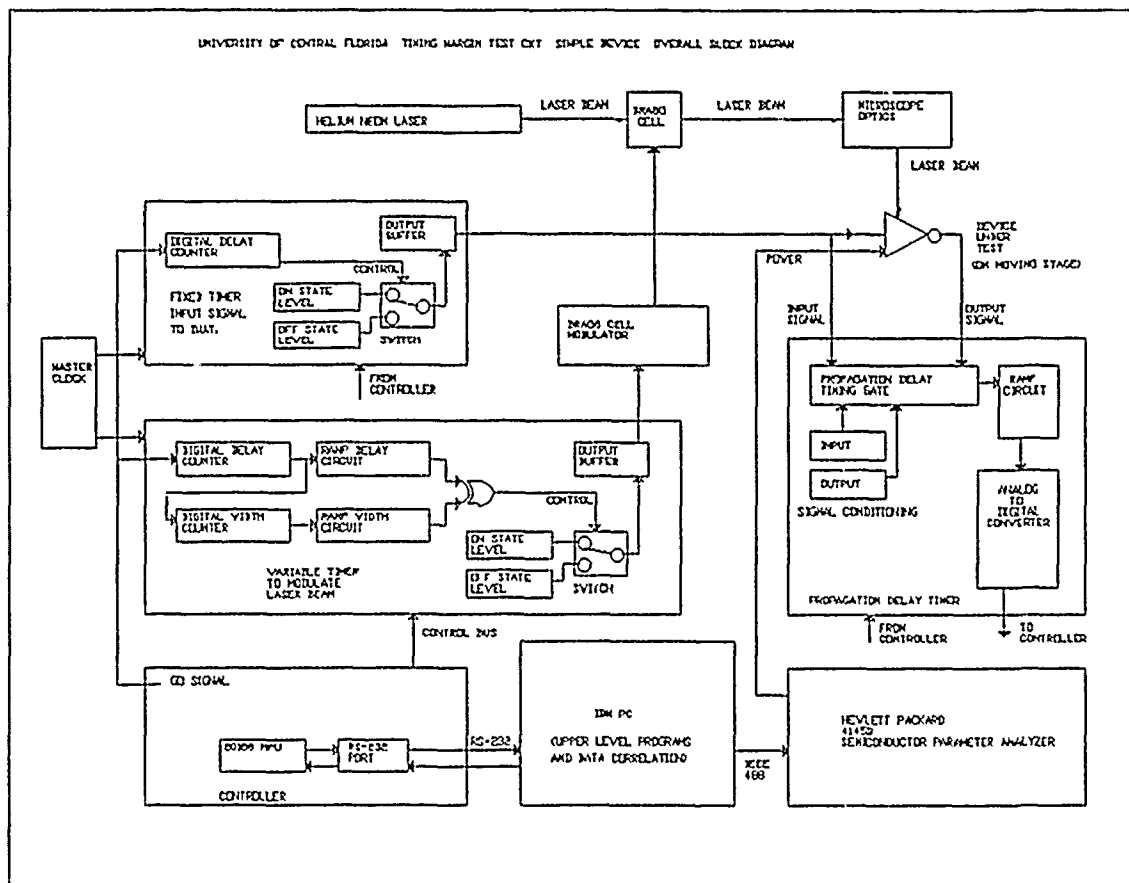
The unbuffered and buffered inverter are tested using this plan. This circuitry measures the properties of a CMOS inverter subjected to laser illumination. A test sequence uses two timers to determine when to illuminate a DUT when the input of the DUT changes state. After the illumination, the propagation delay circuit will have contained a value which is recorded in controller memory, and then all of the timer equipment is reset.

The circuit has two timers, one to give the device under test (DUT) an input signal, and the other to time the laser pulse. The propagation delay is measured by a third timer that has inputs connected to the input and output of the DUT. The test setup, with the controllers and computers, is shown below.

Notice the various circuits in each timer block. They comprise a digital and a ramp section driving a multipurpose output configuration. These will be discussed in depth later.

Controller

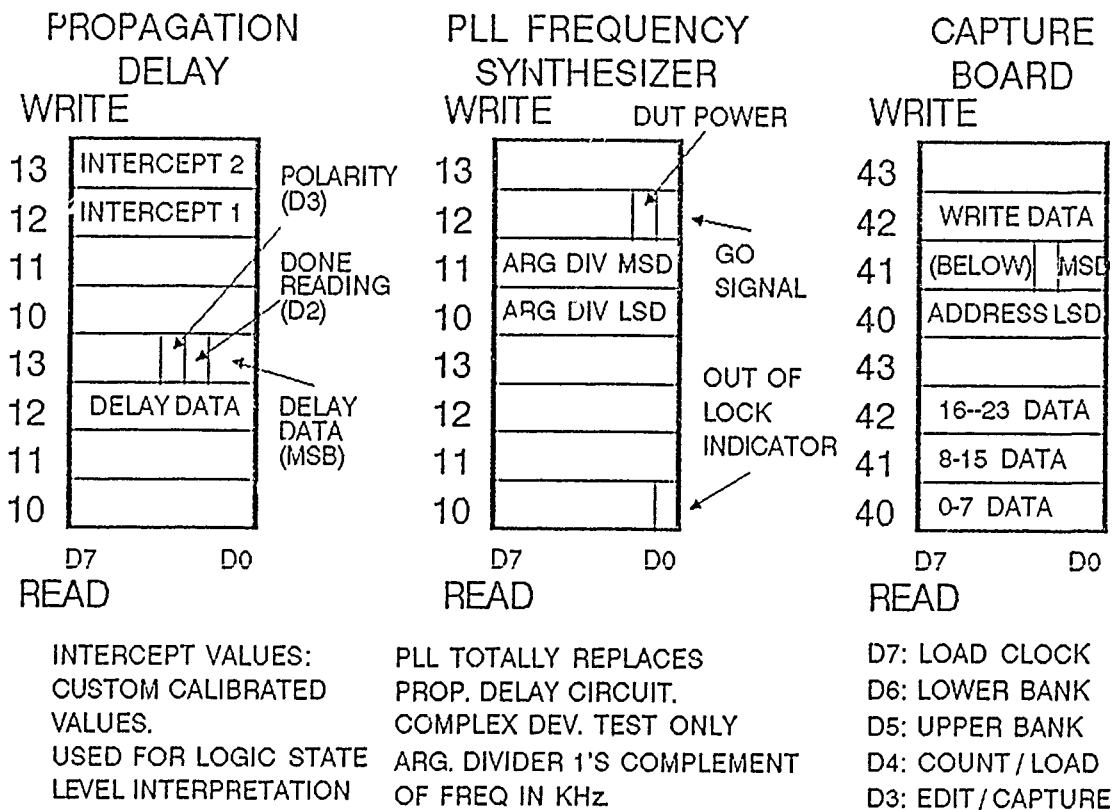
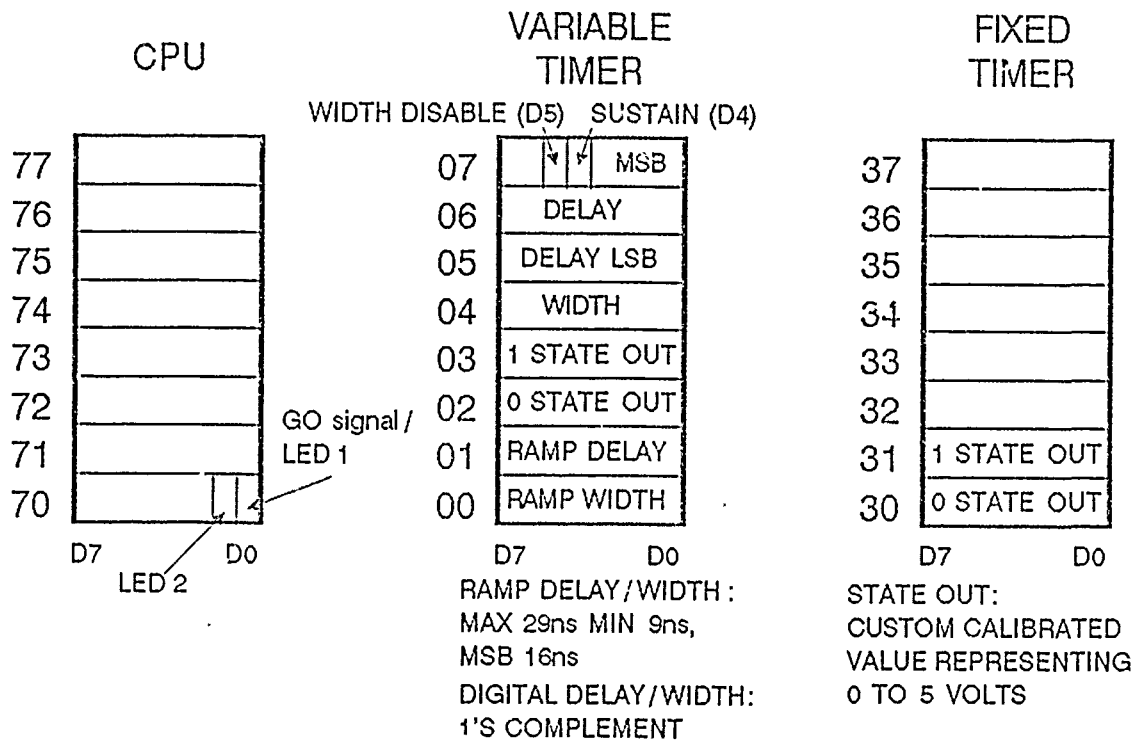
This circuit uses an 80188 embedded controller chip to operate the test bed electronics. This chip has a IO/memory controller, an interrupt controller, a DMA controller, and timers integrated with the microprocessor. Except for a set of registers at the top FFxx and FExx of the I/O map that configure the 80188, the behavior is identical to the 8088 chip used in the IBM PC. The memory/IO handler was the only peripheral 80188 circuit used.



The memory and IO maps are shown below. The register organization for all of the circuits except the 8250 UART are also shown.

IO chip select 1 is decoded by an LS138 to form decoded chip selects to go through the card bus which are further decoded by more LS138's to direct data to individual registers on the cards. IO chip select 0 goes to the 8250 Asynchronous (RS-232) Communications Interface. IO chip select 2 is connected to the card bus for any needed future use.

REGISTER SET MAP

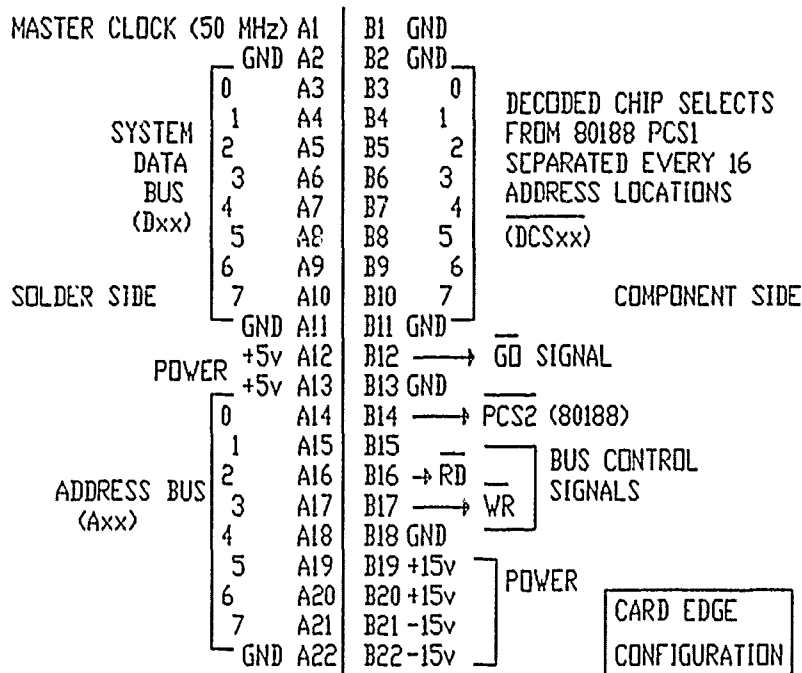


Extra circuitry on the controller board sends a GO signal (a time-controlled signal to start a test) to the card bus to operate the three timers. The signal is latched onto an LS374 and then goes through two AS74 D flip flops to guarantee that the GO signal occurs synchronized with the master clock. This GO signal circuit is used only for the simple device test. The complex device test uses a different signal for the GO signal.

The 8250 is an asynchronous communications controller. It enables the 80188 to talk to the IBM PC through a serial port. MC1488 and '1489 drivers and receivers translate the bipolar voltage of the RS-232 port to common logic signals for the 8250. Only the data wires are used in this communications link. All modem control and status lines are not used. No strict handshake is used for data communication, but data is verified using checksums. The 8250 has a separate 1.8432 MHz crystal for its clock, although it could accurately operate off the 3.072 MHz signal off of the 80188. The separate crystal was used to enable code compatibility with some IBM PC software.

Card Bus

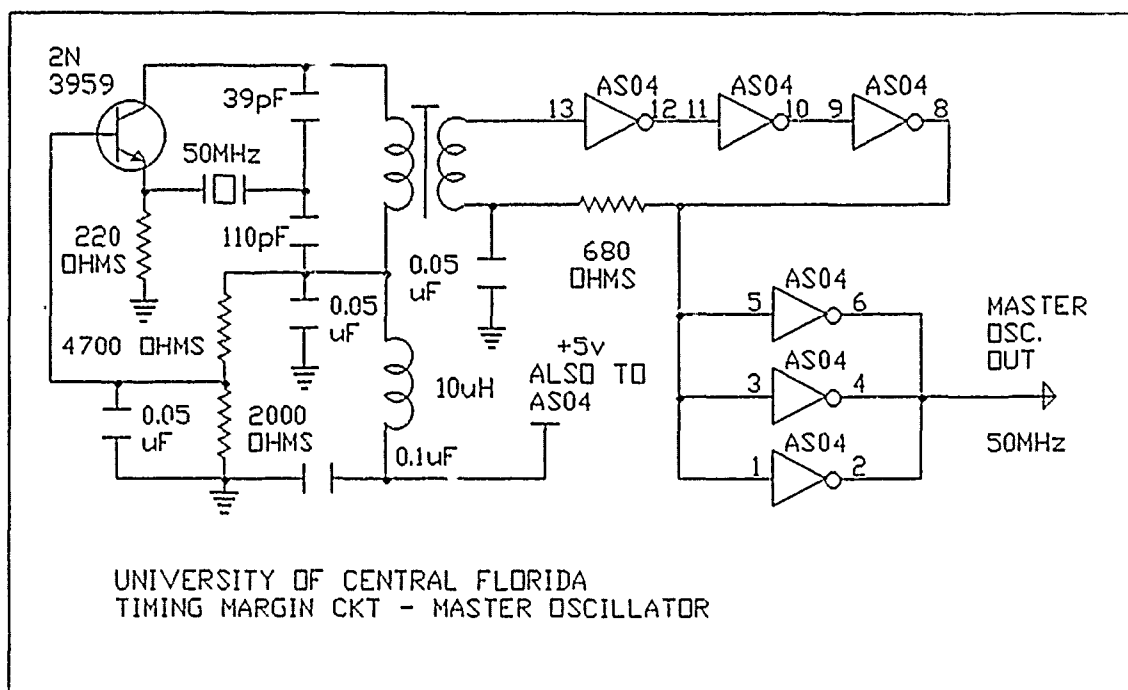
The card bus is a pure parallel 44 pin .158 inch spacing double sided socket bus. Heavy wires are connected in a grid format to form a ground plane, and are especially used around the master clock, GO and +5v power signals. All card slots will accept all cards. This bus was developed to enable interchanging cards for the simple and complex device test plans without rewiring the connections between the cards. The edge connector configurations for all of the cards is shown below.



Master Oscillator

This oscillator generates the 50 MHz signal used throughout the timer circuitry. This signal is the one ultimately responsible for synchronizing the fixed and variable (laser) timers and for giving the digitization of both their accuracy. It is also responsible for giving accuracy to the phase locked loop in the complex clock plan.

The oscillator is a crystal controlled resistive Colpitts oscillator with frequency primarily determined by 50MHz 5th overtone crystal and somewhat determined by the transformer that couples the energy into the inverter chain. An inductor-capacitor combination decouples the oscillator power supply from the noisy digital supply. Three inverters form a saturating analog amplifier with a gain of approximately 150 to create a solid digital signal from the oscillator. The other three inverters buffer the signal for use in the card bus.



Fixed Timer

Since the variable timer handles all absolute variable laser delays, and thus all relative delays between the DUT input signal and the laser pulse, no such variable delays are needed in this timer. This timer presents only the delay needed to ensure that the variable timer can delay enough before and after the signal presented by the fixed timer. The Bragg cell driver delays the laser gate signal by about 200 nanoseconds, and the laser signal must occur 100 nanoseconds before the DUT input signal on some tests. This is 300 nanoseconds and must be matched by the fixed timer. The fixed timer provides 520 nanoseconds of delay, giving the variable timer a 220 nanosecond margin. This margin can be precisely compensated for in software, so that the coincidental happening of an input signal and a laser pulse will correspond to a 0 nanosecond software delay.

This timer needs to provide only a rising or falling edge: no pulse with a width is needed. The output will be one such state before the 520 nanosecond delay is concluded, at which time, it will transfer to the other state. It is able to properly output to a DUT that operates on supply rails between 2 and 5 volts, calling for a logic programmable outputs.

The fixed 520 nanosecond delay is accomplished by the two AS163's to the left of the schematic. When the test is on standby (GO signal LOW,) the counters are held in a LOAD state, where the data loaded is the 2's complement (inverted signal + 1) of 26. At the master clock signal after the GO signal goes HIGH, the counters begin their count sequence

upward until the counters have reached an output of all 1's (FF hex), when circuitry including an AS30 sends a signal to the AS163's which prevents them from further counting. This in effect terminally freezes the counters and terminates the delay. The signal that freezes the counters is also processed through a 10231 ECL D flip flop (center of FTMR schematic in the next appendix) to clean up any AS163 inconsistencies. This signal is the end-of-delay state change signal. The GO signal remains active until the end of a test sequence, at which time it will go LOW and immediately place the counters in the LOAD state. The entire counter circuit, including the 10231, will delay the GO signal by 26 master clock cycles. Since each cycle of the 50 MHz master clock is 20 nanoseconds, the total delay is 520 nanoseconds.

The AS163's have their ripple enable lines connected so that all counters above the least significant nibble (4 bits) can clear all of their ripple carry lines within 16 clock cycles, rather than 1 clock cycle. All of these counters are allowed to toggle in parallel during the carry of the least significant counter only. This allows 16 times as much time for the ripple carry to settle than the conventional scheme of connecting the ripple carries of the counters to the ripple enables of the next counters. The AS163's for the 20 bit counter in the variable timer would have a maximum operating frequency of 30 MHz had it not been for this scheme. Now it has a maximum operating frequency in the 75 MHz range, enough for the 50 MHz master clock. Any operations involving changing global states in the counter, such as freezing count or automatically loading the counters usually involve many gate delays and it is desired to shorten these delays as much as possible. A simple approach is to AND the most significant and least significant counter ripple carries to form a special "end of count" signal. This is effective if the "end of count" signal is all "1"s. This is true for all counters in both test plan circuits. This technique is used in the phase locked loop counters in the complex device test circuit. A higher performance, but more critical approach is to AND all of the output signals (Q0 - Q3) of the least significant counter with the ripple carry of the most significant counter. This gives about a 3 nanosecond improvement over the other technique, but requires the AND gate to be physically very close to the counters to reduce switching noise. This technique is used in both the fixed and variable timers.

The general purpose output signal scenario is realized by the circuitry on the right of the schematic. Two current sinks that can be varied so that the resultant output voltage is between 0 and 5 volts are formed by DAC-08's which are on the bottom right of the schematic. These circuits receive signals from the controller latched by the

LS374's on the bottom. An LS138 addresses the latches. These received signals control the sink currents. The current sinks are connected to a Gilbert cell multiplier configured to be a single pole double throw current switch. The control signals to this switch come from the 10231. These are balanced ECL type signals. They are voltage translated by sets of three diodes to fit the input voltage requirements of the Gilbert cell. Depending on whether or not a state change has come from the timer (if it has been 520 nanoseconds or not), one or the other current sink will be connected to the output buffer. This enables the output voltage to be any state at any voltage for both times (before and after 520 nanoseconds.) Any current needed by the switch transistors in one state is balanced by the current requirements in the other state by use of matched transistors in the single chip Gilbert Cell circuit.

The output buffer consists of a current amplifier, a current to voltage converter, and a voltage follower. It is on the top right of the schematic and is also shown on the next page.

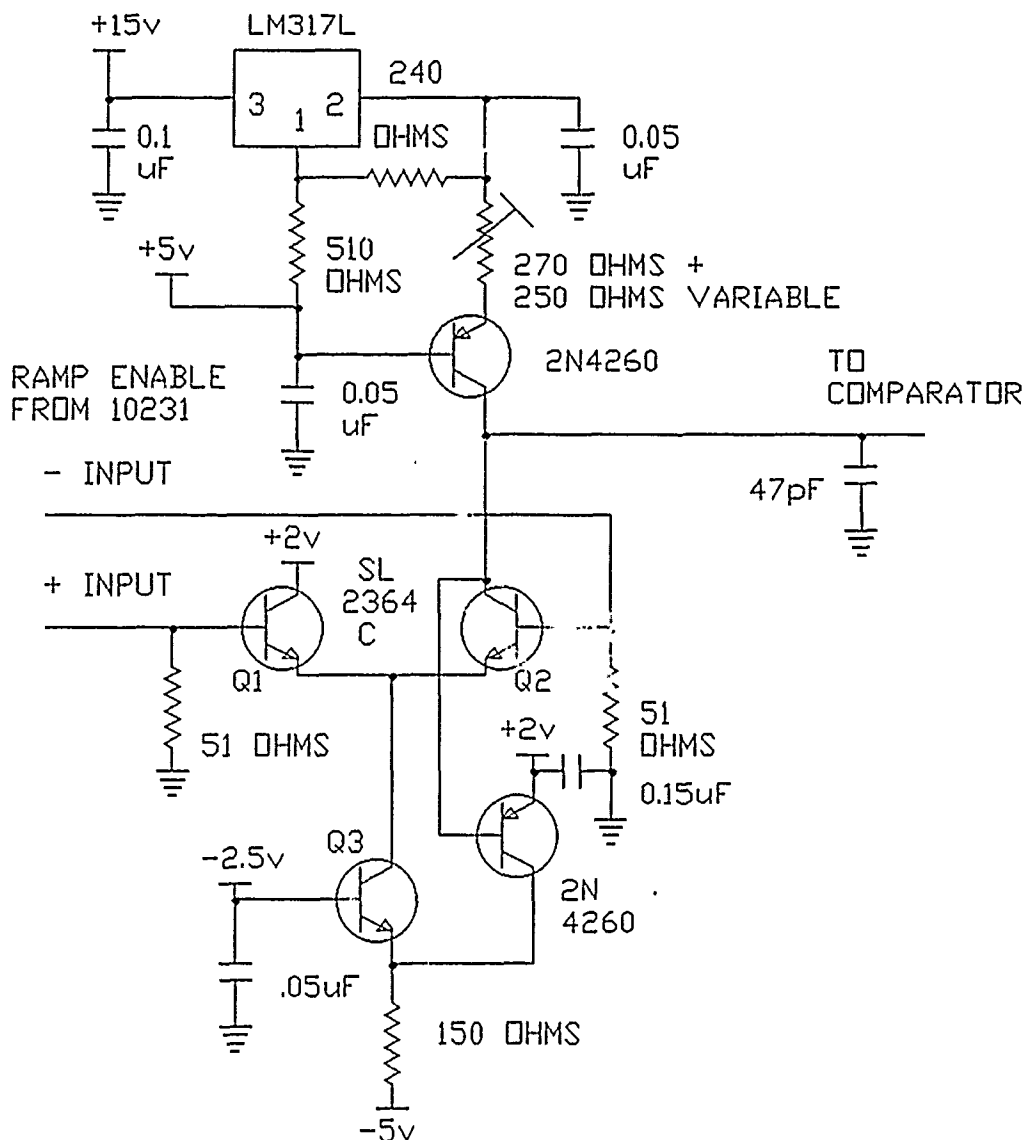
The two transistors on the left are configured as a cascode amplifier, and have very low collector capacitance by because the cascode design cancels any Miller capacitance between the base and collector of the second transistor. The current from the Gilbert cell is converted to a voltage by the two immediate base resistors (180 and 1500 ohms) and then back to a current by the 33 ohm emitter resistor of the lower transistor. The diode in the emitter circuit was added to better define the emitter resistance and to provide temperature compensation to the cascode amplifier.

This timer controls the laser. It must delay a specified delay, and then, after changing output state, delay for a pulse width, after which the output state returns to the initial state. It is composed of two digital timers followed by two ramp timers. The digital timers are built along the same lines as the fixed timer, except the values received in the AS163's during LOAD state come from the controller and are latched by LS374's controlled by an LS138. To get a known delay, the value presented on the counters must be the two's complement of the delay divided by 20 nanoseconds. Therefore, to get a delay of 500 nanoseconds out of the counter, the two's complement of 25 must be presented to the counter. The digital timers are capable of accurately timing to 20 milliseconds of delay and 5 microseconds of width.

Any residual delay needed from the timer (0 to 20 nanoseconds) is handled in ramp circuits. A ramp circuit charges a known capacitance with a known constant current after the 10231 signals so. After a time the voltage, which has been increasing linearly, passes a known voltage point. When this happens, a comparator causes subsequent logic to change state, thus altering the output state in the same way that the output state had been altered in the fixed timer. The ramp circuits have a coarse adjustment range (1 nanosecond increments out of 30 nanoseconds) to lessen any noise effects in the analog ramp circuits.

The charge pump circuitry for the ramp circuit is shown on the next page.

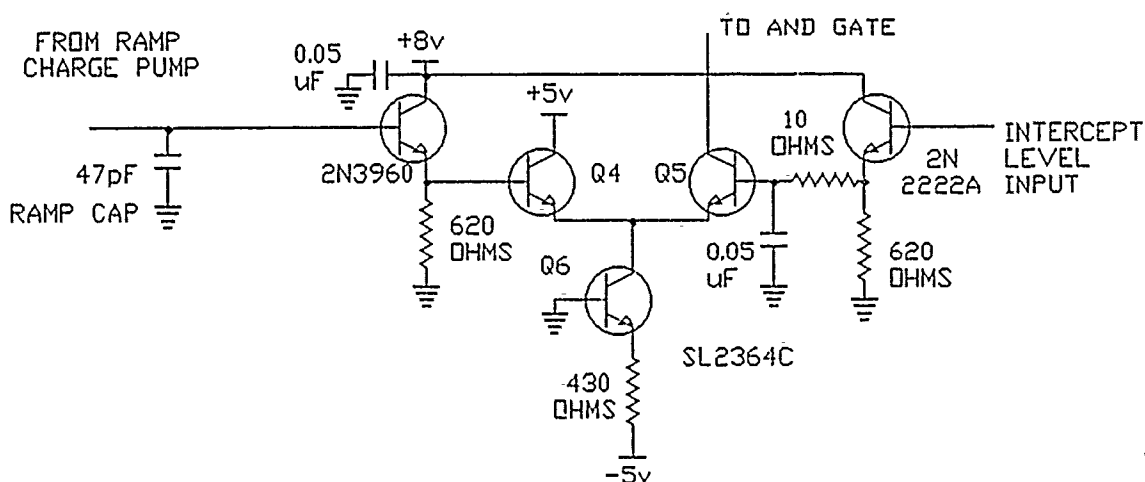
It operates on the principle that the sink current from the ramp capacitor is greater than the source current when the ramp circuit is in reset. Q2 is conducting and Q1 is not conducting when the circuit is in reset. (Q1, Q2 and Q3 are on one chip, the Plessey SL2364C.) The PNP transistor (2N4260) prevents Q2 from saturating by stealing current from Q3 (and therefore Q2) to the point that the remaining current equals that of the current source. The circuit also prevents the PNP transistor from saturating by forcing its collector voltage to be below -2.5 volts during the current stealing operation. The four transistors need to operate in the linear mode to enable the circuit to come out of reset mode fast (1 nanosecond, according to measurements.)



When it comes out of reset, it does so at the end of the digital timeout and so that Q1 conducts, shunting the sink current to ground, and also so that Q2 does not conduct, disconnecting the sink current from the ramp capacitor (the 47 pF capacitor to the right.) The capacitor is now free to charge from the constant current source, which is a second PNP transistor and a LM317 regulator. These two parts are connected so that the regulator will track the +5 volt supply, controlling the voltage difference between emitter and base of the current source transistor, thereby making the output current insensitive to power supply variations. A variable resistor in the emitter circuit adjusts the output current. The result of this charge pump and capacitor arrangement is a positive slope ramp starting at a known voltage at a known time (end of digital counting) and ramping up linearly until the voltage is within the voltages of the current source transistor. Saturating this

transistor makes no difference in timing, as the test setup takes about 10 microseconds to reset, and this transistor would have unsaturated by then.

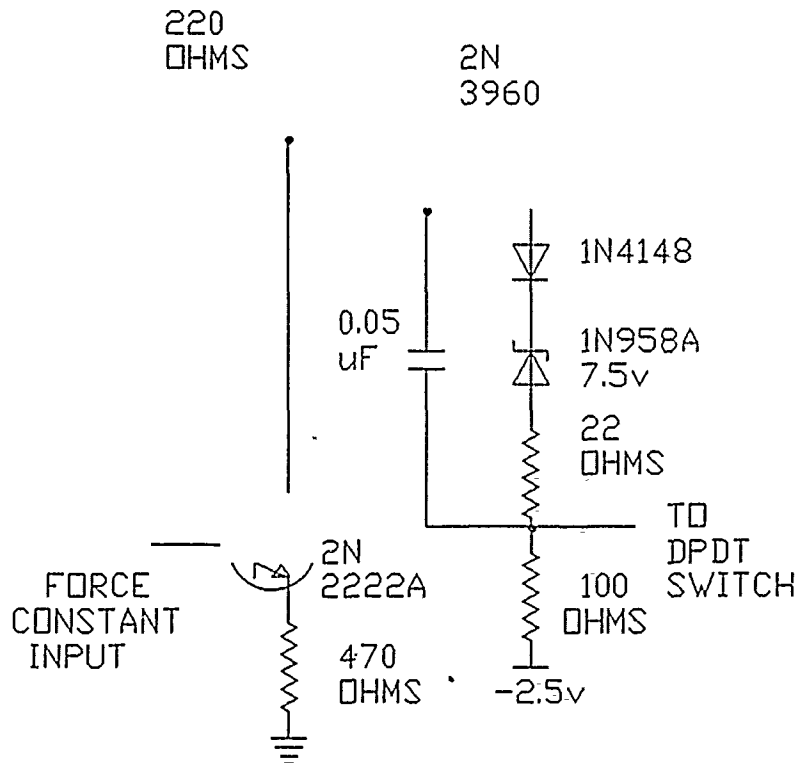
The comparator determines when the ramp exceeds a certain level. This level is determined by data from the controller and is converted from a digital signal to an analog signal by DAC-08's at the bottom left of the main ramp circuit schematic. If more delay is required, this intercept level is made higher; if less delay is required, this intercept level is lowered. The comparator circuit is shown on the next page.



The 2N3960 and 2N2222A on both sides of the comparator isolate the high impedance circuitry of the ramp capacitor and the intercept current to voltage converter (the 2.2k resistor at the base of the 2N2222A) from the comparator. Similar resistances (620 ohm) on the emitters of both transistors assist in cancelling nonlinearities presented by these transistors to their high impedance sources. The 0.05uF capacitor isolates the comparator from noise on the intercept level line, and the 10 ohm resistor is to enable the 2N2222A transistor to survive large voltage changes on this intercept line. The 2.2k resistor on the base of the 2N2222A and resistors feeding current into the DAC-08's are connected to a stable 5.5 volt reference to make the intercept circuitry insensitive to power supply variations.

The comparator is a difference pair with "long tail" transistor (Q6) base connected to ground to reduce Miller capacitance effects at the emitter junction of the difference pair. Gain in the comparator is sacrificed for speed. Since the delay adjustment resolution is rather coarse (above), gain is not critical. The comparator is connected so that the collector to the wired NAND gate sinks current when the delay timer is reset, and does NOT sink current to the wired NAND gate when the width timer is reset.

The logic circuit (below) consists of a partial exclusive OR gate (an AND gate), an OR gate, and level shifting circuitry.

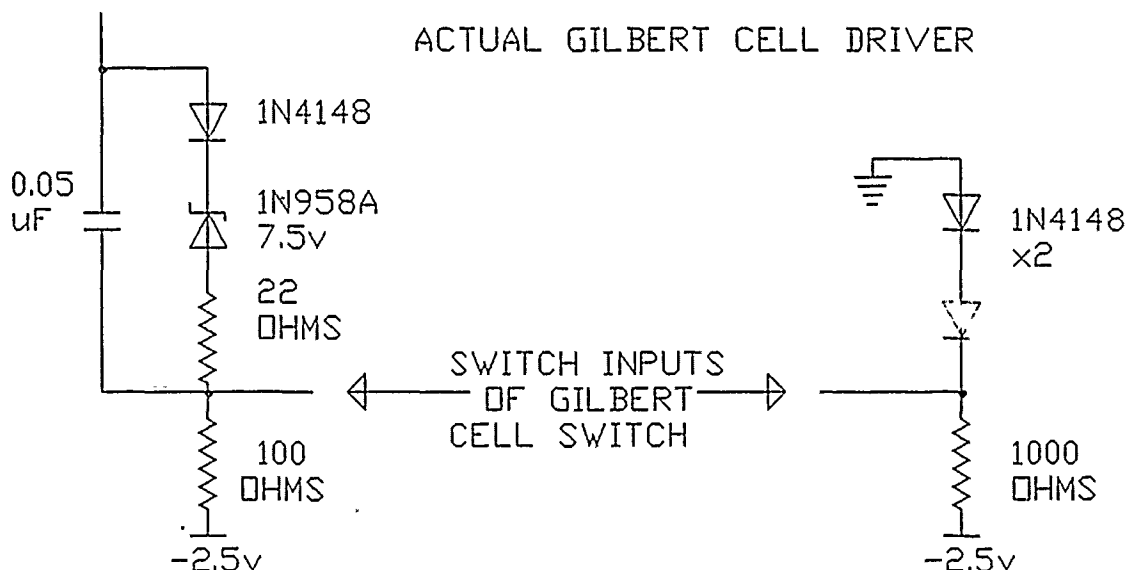


The signals from the two comparators are AND'ed together at the base of the first 2N3960 transistor and 220 ohm resistor. The signals from the comparators are arranged so that the 220 ohm resistor sees no current (and therefore put a logic HIGH on the transistor) when the delay ramp has passed the intercept, but the width ramp has not. This corresponds to the time when the pulse is active. This voltage is wire OR'ed with a voltage from the "force active" (or "force constant") input (active LOW) processed by a 2N2222A transistor, a 2N3960 transistor, and two resistors. This signal forces the output state to be the same as the state when the pulse is active. The output of the OR gate is then level shifted by a zener diode from the +7 volts of the OR gate to -1 volt required to operate the Gilbert cell SPDT switch, identical to that of the fixed timer. The 1N4148 diode in series thermally compensates the zener diode, the 0.05 uF capacitor bypasses the voltage dropping at high frequencies, and the 22 ohm resistor works with the 100 ohm load resistor to tweak the input range of the Gilbert cell. This resistor is not mentioned on the main ramp circuit schematic, but is preferred for maximum

performance. It is guessed that if these circuits were repeated, different resistors might be used to tweak this circuit. Much better is a design that outputs a difference signal from the OR gate to the Gilbert cell, because then such tweaking resistors would be unnecessary, but this was not implemented in this design. The actual circuit and the preferred circuit are shown on the next page.

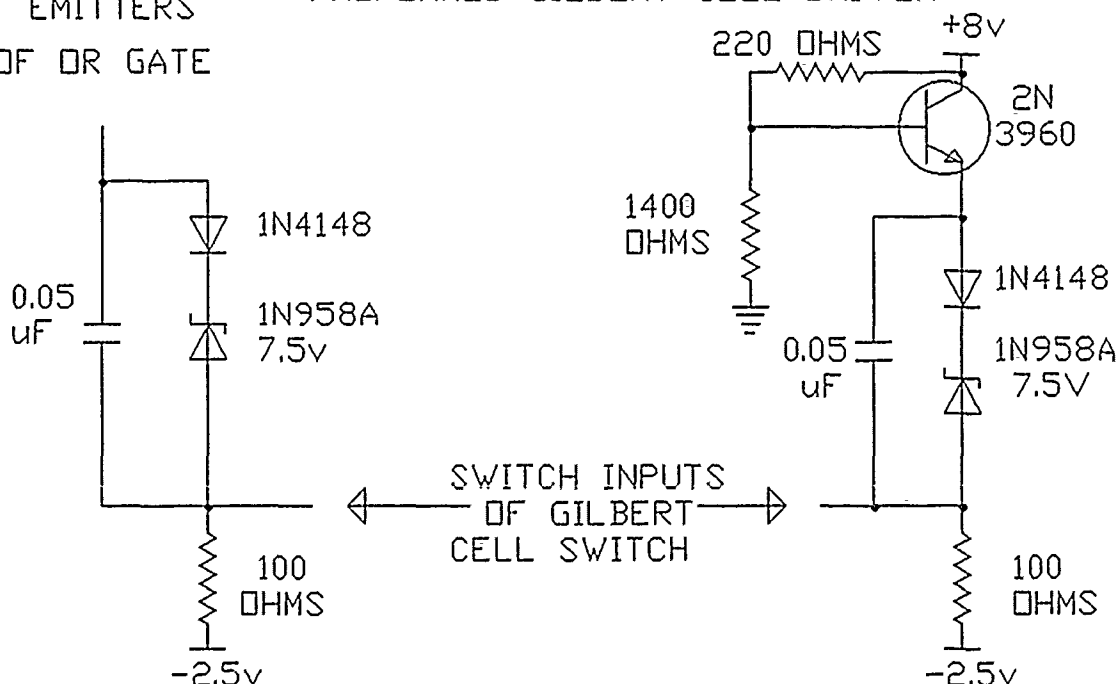
EMITTERS
OF OR GATE

ACTUAL GILBERT CELL DRIVER



EMITTERS
OF OR GATE

PREFERRED GILBERT CELL DRIVER



[illegible]

Propagation Delay Measurement

The input signals from the DUT are buffered by accelerated emitter followers after travelling a maximum of six inches of low capacitance constructed cable. The buffered signals go to voltage comparators consisting of PNP differential pairs with PNP long tails that have their bases connected to AC ground to reduce Miller capacitances. The reference levels for the comparators are signals from the controller converted to analog signals by DAC-08's and buffered by 2N2222A's in the same way that the levels in the variable timer ramp circuits are processed. The 620 ohm resistors at the bases of the comparator transistors help in reducing nonlinearities in the same way that they reduce nonlinearities in the variable timer ramp circuit.

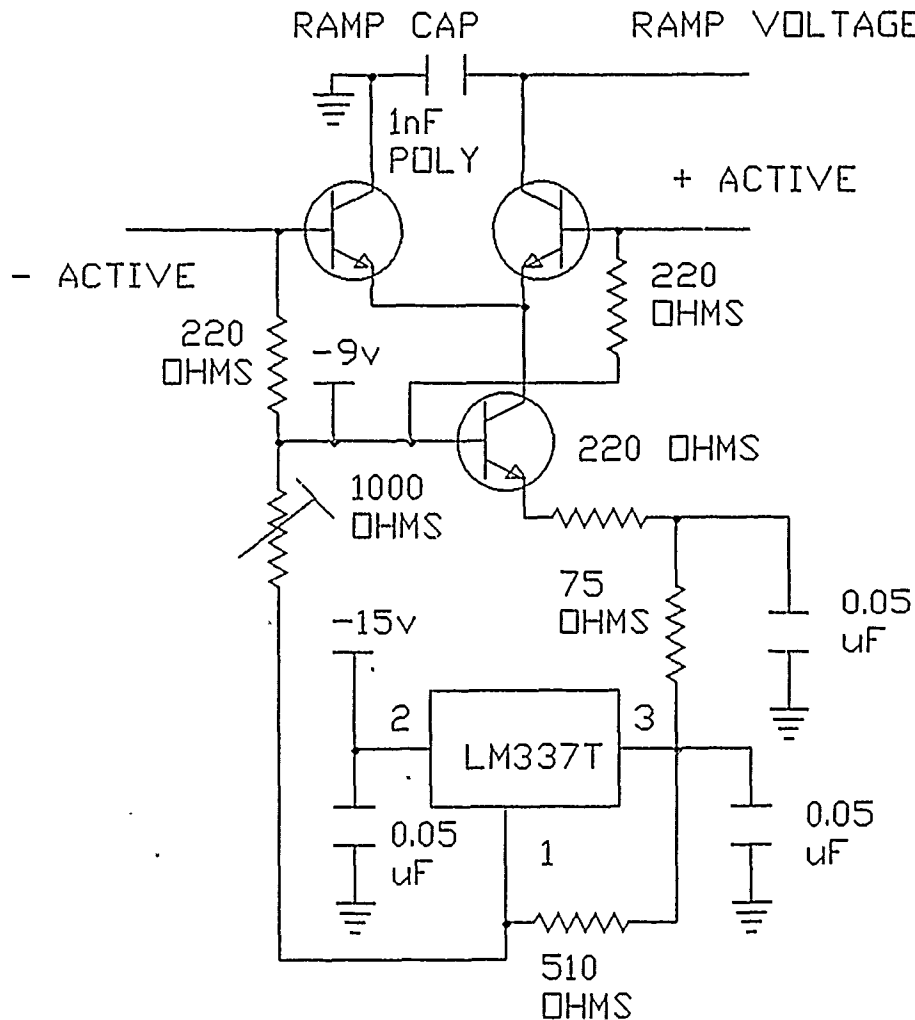
192

outputs signal if both inputs are high or if both inputs are low. If the input to the DUT was a rising edge, then the first Gilbert cell output would signal a normal delay; if the input to the DUT was a falling edge, then the second output from the Gilbert cell would signal a normal delay. Outputs opposite of above would signal an output transition (caused by the laser) that happened before the input transition. Both outputs are inactive when the inverter is in a quiescent state. These two outputs are decidedly latched by an RS flip flop composed of AS00 gates.

The outputs of the other Gilbert cell are merely connected together to form a true exclusive OR function. The exclusive NOR (equivalence) function is obtained by reversing the balanced outputs of the Gilbert cell. Therefore, the output of the Gilbert cell is active only when both inputs from the DUT are the same value. This corresponds to the time between inverter transitions, or the time at which the propagation delay is measured.

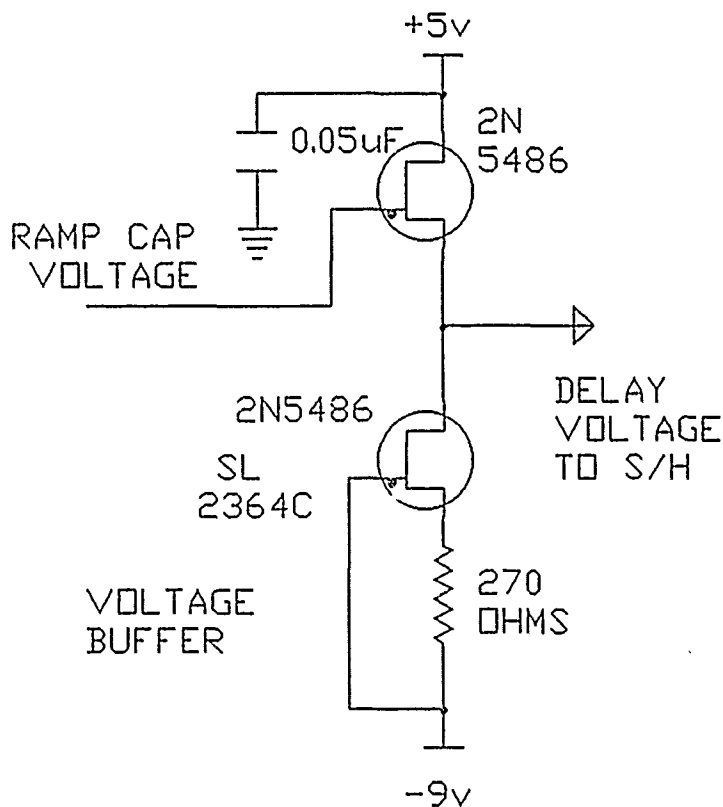
The output of the Gilbert cell is emitter follower buffered and level translated to a negative voltage (-8v) by zener diodes to operate a single pole single throw (SPST) switch formed from a difference pair on a Plessey chip. This switch connects a .001uF (1nF) polystyrene capacitor to a current sink formed by the long tail transistor in the switch pair and a LM337 regulator, only when the Gilbert cell indicates an active output. The current sink operates in the same way that the current source operates in the variable timer ramp circuit, except the current adjustment changes the regulated voltage across the constant current sink emitter resistor. The emitter resistor, composed of 220 ohm and 75 ohm resistors, has a constant value. The switch and current sink is shown in the middle of the ramp schematic for the propagation delay timer and is reproduced below.

RAMP SWITCH CIRCUIT



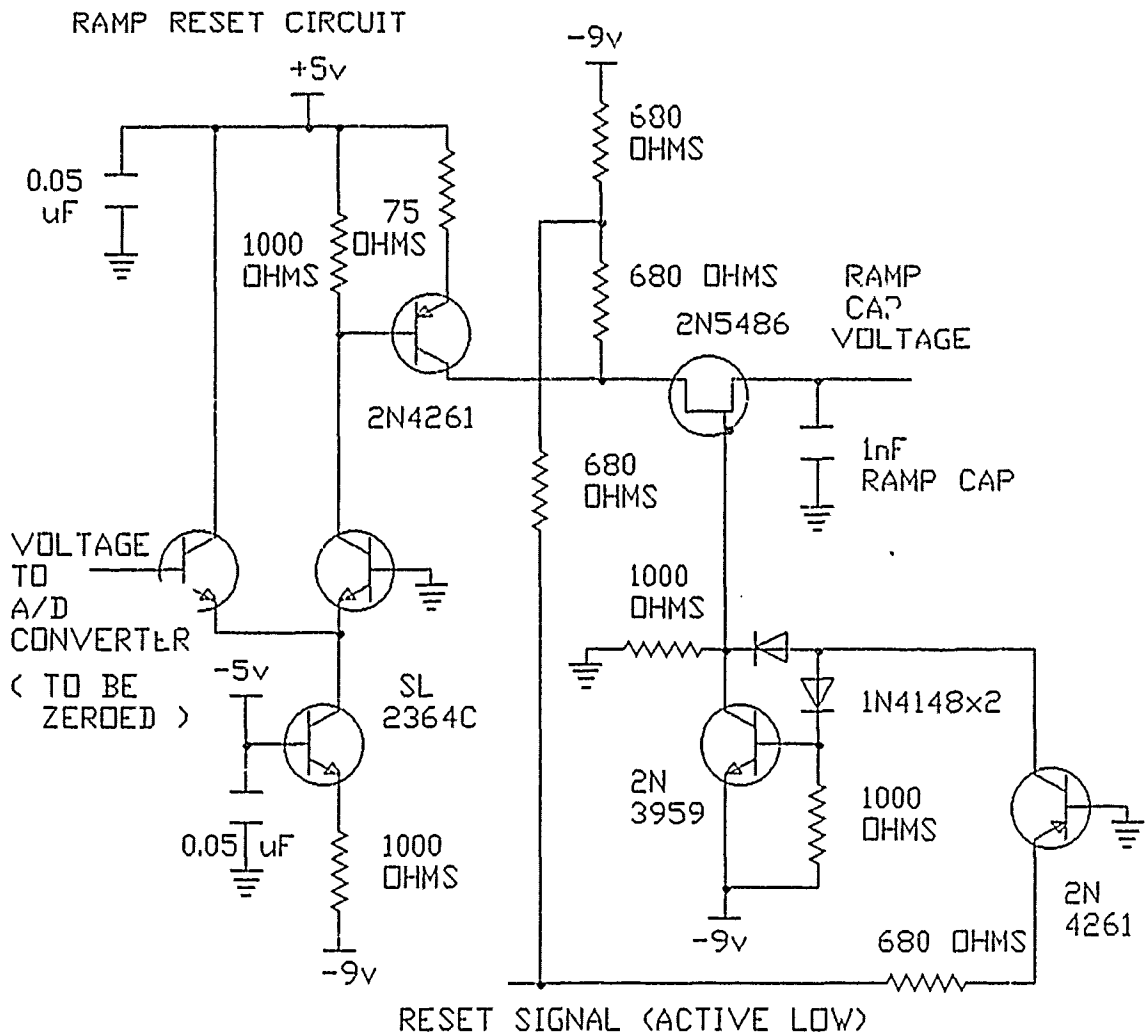
The rest of the circuitry is a high impedance buffer to the ramp circuit and a circuit to force the buffer output of the ramp circuit to zero when reset.

The ramp buffer is a pair of FET's connected as a constant voltage rise high impedance source follower. The lower FET is connected as a constant current sink to linearize the source follower (upper) transistor. This circuit is shown below.



The reset zeroing circuit is a differential pair with PNP transistor configured as an operational amplifier. The noninverting input is tied to ground and the inverting input is tied to the signal wire connected to the ADC (analog to digital converter.) The negative feedback loop is completed when the FET connects the OP AMP output to the ramp capacitor. The ramp capacitor will then charge to some (negative) value to maintain the output of the buffer described above at zero volts. Whether the capacitor is at zero volts or some other value makes no difference to the ramp switch, as it only operates with differences of voltages. When the FET opens, the capacitor will remain at that preset voltage, forcing the buffer output to remain at zero volts. The reset (active LOW) signal at the bottom of the schematic below goes to two locations. The first location is a PNP common base translator and an NPN common emitter switch with Baker clamp (two diodes), both used to translate a TTL level input to an output suitable for driving the FET. The other signal goes to a matrix of 680 ohm resistors acting as the load line for the PNP transistor in the OP AMP. The matrix reduces any voltage variations due to the FET slowly opening, especially due to the rapid current transitions of the PNP transistor in the OP AMP and the capacitance in the FET.

The Sample Hold chip (AD580) grabs the voltage off of the ramp circuit when all delay testing is finished, and stores it on a capacitor (100pF) for use by the ADC (analog to digital converter.) The ADC then converts this voltage (after being zeroed and scaled by two trimming resistors) to a 10 bit digital value to be read by the controller. The ADC (ADC80) is a 12 bit successive approximation converter that takes approximately 30 microseconds to make the



conversion. Only the most significant 10 bits are used as data; the other two bits are too noisy to resolve.

The sequencer (on the ADC schematic) is a chain of inverters and timing components used to properly sequence all operations on the propagation delay capture board. The first delay circuit is a fixed 6 microsecond delay to tell the sample hold circuit to hold the ramp voltage. Before that, the GO signal goes directly to the ramp circuit to immediately unreset it so that it can accept a propagation delay. The 6 microsecond delay circuit is composed of a 22K resistor and a 1500pF capacitor. The timing signal is

further delayed by 1.5 microseconds (12K and 1000 pF) to tell the ADC to begin conversion, after the sample hold has settled. The actual signal that begins conversion is a 500 nanosecond wide pulse generated by a pulsing circuit using a 4.7K resistor and a 390 pF capacitor and sent to the ADC. While the pulsing circuit is operating, another delay circuit begins operation to delay the timing signal by 38 microseconds, enough to cover the time that the ADC makes a conversion. The timing components on it are a 1100pF capacitor and a 56K resistor. The output of this timer goes to the controller to signal when the data is gathered and the conversion is done. When the GO signal goes inactive, then the ramp circuit immediately resets, the sample hold immediately goes into sample mode, and the conversion flag immediately goes inactive. No signal goes to the ADC.

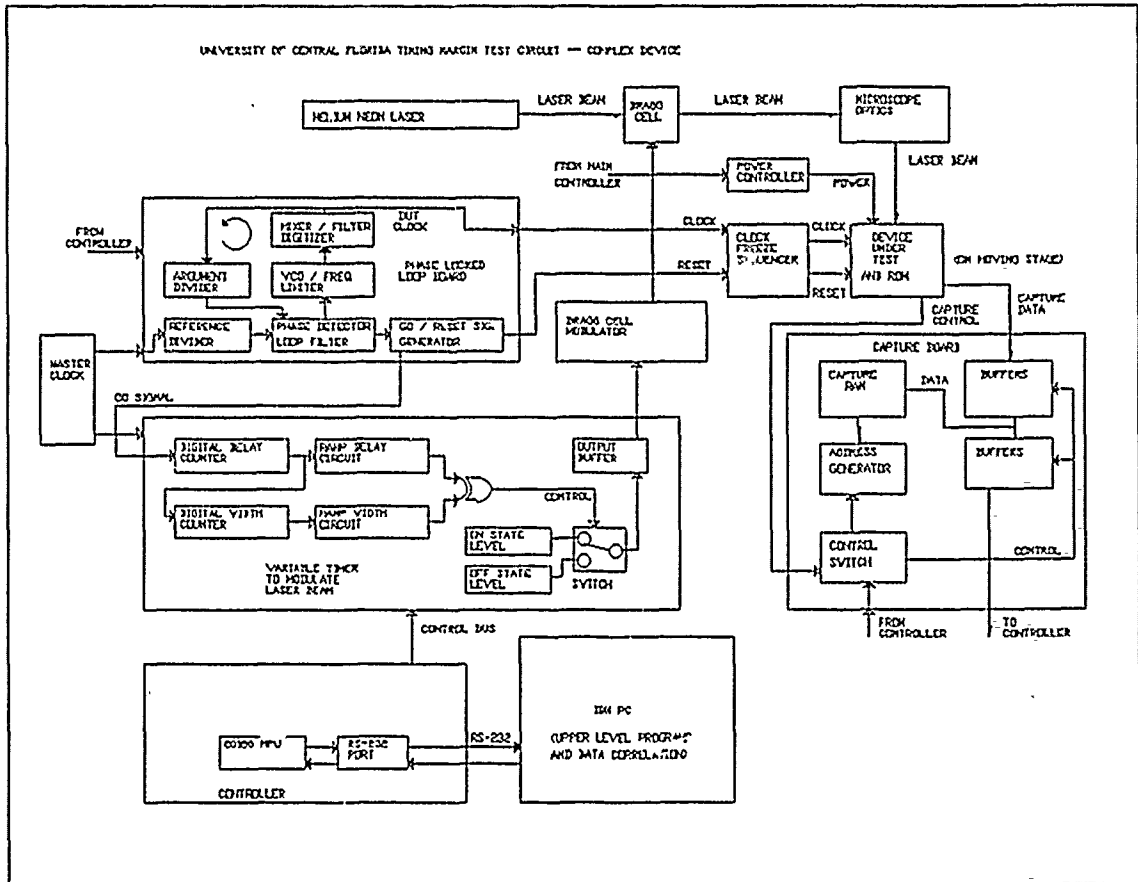
Complex Device Test Plan

The microprocessors are tested in this plan. This test involves finding the timing margin, or at least the amount of "criticality" as a figure of merit, to several nodes in the complex device. The complex device test involves three parts: finding the nodes with any fault in them, ranking these nodes with regard to how critical they are, and doing a state rank, where certain "states" or conditions of operation within the complex device are tested and ranked.

Three extra circuits are introduced in this test plan. Whether any of these three are used depends on the three parts of the test plan described above. The first circuit is a phase locked loop frequency synthesizer. It is used for all complex device tests, as it is responsible for generating the clock for the complex DUT. The second circuit is a capture memory. It records all test results from the DUT and is also used in all aspects of the complex device test. The third circuit is a sequencer and is used only for state ranking, although it is in operation for all complex device tests. It coordinates the laser timer to the internal logical states within the DUT. It calls on help from the DUT, PLL (phase locked loop), and the laser timer to coordinate timing between the laser and DUT. This circuit has no effect on the first two aspects of the complex device test, as the timing functions of the laser timer are disabled, and the laser operates continuously. The block diagram to the complex device test circuit is shown on the next page.

Controller

The controller is the same as the controller for the simple device test plan, except that the GO signal to the lower right



of the schematic is disconnected, and the code in the ROM is different. Actually the same card is used in the same bus that was used for the simple device test plan. The master oscillator is still used as a stable reference in the complex device test circuit. The variable timer and PLL need its frequency.

Variable Timer

The variable timer is unchanged from the simple device test. A 9-pole filter is connected across the output of the timer during node find and node rank (both needing only continuous illumination) to reduce noise coming from the timer. This filter has follows no classic configuration, except that it blocks frequencies above 50 kHz. These tests are very sensitive and any noise reduction is appreciated. The filter is disconnected during state rank, so that the needed nanosecond pulses can go to the Bragg cell (laser modulator) without hindrance.

The fixed timer is not needed for the complex device test. It is merely excluded from the complex device test circuit.

Phase Locked Loop

This circuit synthesizes the clock frequency for the DUT. It also aids in coordinating the DUT and laser timer. It is a standard radio frequency synthesizer phase locked loop with conversion required to get the wide 2 to 50 MHz range. All methods applied to phase locked loop operation apply here.

The phase locked loop operates on the principle that an oscillator will have its frequency and phase changed to match that of a reference signal. Any errors detected by a phase detector will generate an error voltage that will go to correct the oscillator's phase. For the phase detector in this circuit, it is also true that any frequency errors on the phase detector will generate an error voltage that will go to correct the oscillator's frequency. The diagram describing this in the PLL box of the complex device test.

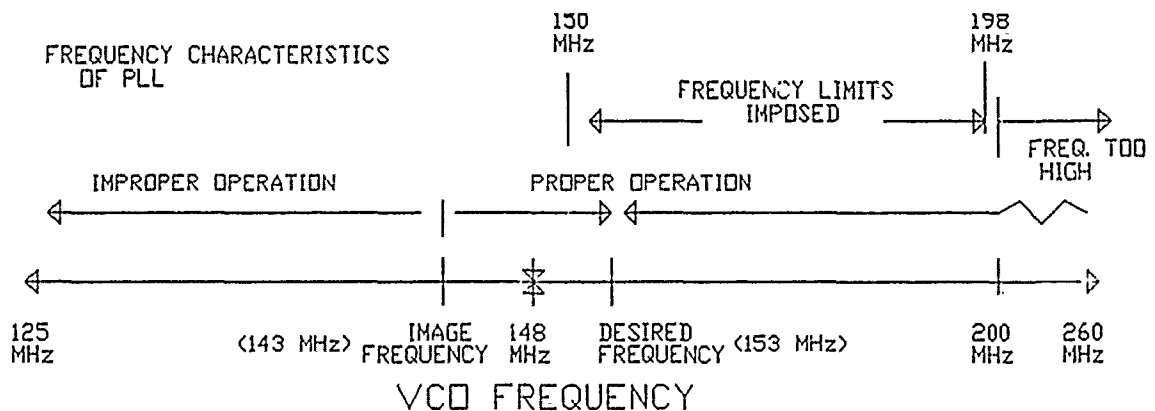
It makes no difference what frequency the oscillator is generating, just so that the frequencies at the phase detector are the same. In other words, the oscillator signal or the reference signal can be divided by any number, and as long as the inputs to the phase detector are the same frequency and phase, the loop will be considered properly locked. This PLL divides the oscillator and reference signals so that the phase detector inputs are both 500 Hz. To use the 50 MHz reference (master oscillator,) the reference frequency would have to be divided by 100,000. The reference divider on the PLL VCO schematic does just this. The argument oscillator (the circuit that actually generates the DUT clock) goes from 2 MHz to 50 MHz. This requires an argument divider range from 4000 to 100,000. The argument divider, located on the CPU interface portion of the PLL schematic does this. The different argument divide ratios are programmed into the argument divider from the controller via LS374's and LS158's. Both the argument and reference dividers operate on the same principles. A number is loaded into a divider circuit when the counter has

all "1"s on its outputs. The counter then counts up, using clock cycles until its outputs are again all "1"s, when the counter again is loaded with the number. The number of clock cycles needed to complete one reload cycle is equated to the divide ratio of the counter. The reference divider gets its load number from hardwired pins (16 bit 2's complement of 50,000 decimal), whereas the argument divider gets its number from LS373's loaded 16 bit 2's complement of the number desired.

The counters in the PLL use the same cascading techniques that are used for the AS163's in the fixed and variable timers. The cascaded AS163 counters operate to a maximum divide ratio of 65536 and output a pulse that is one clock cycle wide. At 50 MHz, this is 20 nanoseconds, and is too narrow to properly operate the MC4044 phase detector. Additional AS163's are therefore connected to the counters to further divide the signals by two and give the MC4044 nice 50 percent duty cycle signals. This division by two doubles the 50,000 divide ratio of the reference divider to the needed 100,000. It also forces the argument divider to divide by even numbers only. The frequency spacing of the synthesizer is the frequency difference produced from adjacent integers going to the argument divider. It is usually the frequency going to the phase detector, or in this case, 500 Hz. But since the argument divider can only divide by even integers, this frequency spacing is doubled, or it is 1000 Hz. The programmed number into the argument divider, therefore, indicates the number of 1000 Hz increments from zero that the DUT clock frequency will be operating at. This programmed number is the DUT clock frequency in kHz.

The circuit actually responsible for generating the output frequency is a parallel tuned Colpitts oscillator using a 1.5 - 11 pF UHF varactor diode for the tuning element. The oscillator has a frequency range between 125 MHz and 260 MHz for a tuning voltage between 0 and 15 volts. This range is limited by five resistors and two diodes to that of 150 MHz and 200 MHz to prevent the loop frequency from going into the negative conversion range, and from going above 50 MHz. Both limits are to enable the PLL to come to a correct and steady lock. The VCO (oscillator above) is heterodyned (frequency convoluted) with a fixed 148MHz oscillator to form the 2 to 50 MHz difference signal. The sum products, also being a product of heterodyning, along with the two oscillator signals are eliminated by a seventh order Chebyshev passive filter. The signal from the filter is amplified by three transistors and then converted to a digital signal by a Schmitt trigger circuit composed of a 74F00, a resistor, and a diode. This digital signal is the clock signal for the DUT and is also the signal going to the argument divider.

Frequency limits are imposed on the 125 to 260 MHz oscillator to assure that the PLL will come to a proper lock. Conditions for not locking otherwise are thus. If the 125 to 260 MHz VCO were to operate below the fixed 148 MHz oscillator, the heterodyne difference signals would be the same as they would be if the VCO operated above the fixed 148 MHz oscillator. The PLL action, however, would be very different. Suppose that a 5 MHz signal is desired from the PLL. If the loop was properly locked, the VCO would be at 153 MHz ($153 \text{ MHz} - 148 \text{ MHz} = 5 \text{ MHz}$.) But suppose that the VCO was operating either below or above 143 MHz, but definitely below 148 MHz. Then two different outcomes would result. If the VCO operated above 143 MHz, then the difference signal would be below 5 MHz needed. The PLL would tell the VCO to increase frequency (actually decreasing it), until the VCO passed through 148 MHz and then coming into convergence at 153 MHz, the proper frequency. Therefore if the VCO was originally operating above 143 MHz, no harm would result. But if the oscillator was originally operating below 143 MHz, then the PLL would tell the VCO to reduce frequency, as the difference would be greater than 5 MHz. This would only serve to increase the difference frequency and further prompt the PLL to reduce frequency, until a point would be reached, where the VCO tuning voltage could go no further, due to limiting in the charge pump transistors or other nonlinear action. This stable point is NOT the proper operating point of the PLL, rather it is some rail sought after from some hysteresis. The voltage to the VCO will then have to be coaxed by external influences to some proper range to get the PLL to operate properly. This action is shown below with the arrows marking the PLL progress to some stable point.



The 143 MHz point described above is the image of the 153 MHz proper operating signal. Notice they are in different directions and the same 5 MHz spacing from the 148 MHz fixed oscillator. If lower frequencies are desired for the DUT clock, then these two points would have to be moved closer together. This places extreme sensitivity on the

lower limit, and as a result for this circuit, dictates a high (2 MHz) limit to be imposed on the DUT frequency, and thus a 150 MHz lower limit on the VCO.

If the VCO is above 200 MHz, the circuitry does not perform as well, as the difference signal would be above 50 MHz. This is caused by general speed problems in the Schmitt trigger and three stage transistor amplifier, as well as involving attenuation in the Chebyshev filter. Therefore, an upper limit is placed on the DUT clock frequency at 50 MHz, and therefore on the VCO at 198 MHz.

The loop filter is a damped single order filter composed of two 2K resistors, a 100 ohm resistor, and a 100uF capacitor. It operates with the charge pump (three transistors on the upper left hand corner of the VCO schematic) to take the error signal from the MC4044 phase detector (on the same schematic) and process it into a control voltage for the VCO and frequency limiters. It is a damped single order filter which makes the PLL a second order negative feedback loop. The other order comes from the frequency-phase integration action of the MC4044 phase detector. The filter parts are selected to give an approximate damping of 0.5 at the DUT frequency of 10 MHz. The damping gets worse at higher frequencies, until around 40 MHz, the loop has locking problems. We did not consider this serious, as the loop is seldom operated above 35 MHz. The damping could have been increased so that the higher frequencies were more stable, but this would destroy the loop characteristics at the more important lower frequencies (2 MHz) as a result of a third order generated within the VCO that is normally negligible at higher frequencies.

The DUT signal phase from the PLL is very stable and predictable with respect to the reference signal phase at two millisecond intervals when the phase detector expects simultaneous rising edges. The AS163 divide by two counters in the reference and argument dividers make this event happen every millisecond rather than every two milliseconds. This phase predictability is used to synchronize the laser timer and DUT.

Capture Board

This board stores the test results from the DUT. It has a 2K by 24 bit fast memory array made faster by pipelining. Three counters and two latches (lower right of capture board schematic) handle the addressing while three buffers and three transceivers (upper left side) handle the data operations. The control inputs to the memory come either from the DUT board or control circuitry on the capture board, decided by an AS158 switch.

The address counters determine what address that the fast memory will be read from or written to. The DUT circuitry will send clock pulses to the address counter when it sends a new data value. When the controller needs a new data value, it also sends a clock pulse to the address counter to update the capture RAM address. The counter is three AS163's connected together in the same way that all of the other AS163 counters are. Their Q (output) lines go to the address lines of the first bank of memory. The second bank gets its address from AS374's connected to the AS163 outputs and clocked on negative edge whereas the AS163's are clocked on positive edge. Therefore, the capture RAM gets data to new addresses on both clock edges. The counters can also be loaded with a number from the controller for aiding in setting the capture RAM address to any arbitrary value. This includes resetting the counter to 0 before the next test sequence.

The data bus contains three AS244's to buffer the data coming from the DUT. When the controller needs access to the capture RAM, the AS244's are disabled (tri stated) and three LS245's are enabled to transfer data to and from the capture RAM. In this way, the data from a test can be read and evaluated, and reset numbers, like 0 or FF hex, can be loaded into memory before the next test. The eight bit reset value loaded into the LS245's from the controller repeat every eight bits (three times) throughout the 24 bit word in memory.

The AS158 in the controller portion of the capture board (including LS138's for controller addressing) decides which set of inputs will control the capture RAM. When the capture board is in Read/Write mode, then the AS158 inputs are directed to the output of a LS374 latch, so that the controller can operate the capture RAM. When the capture board is in Active mode, the control signals come from the DUT circuitry. These four signals are the clock, bank select 1, bank select 2, and write signals. The bank selects and write signal control the memory directly. The clock signal goes to the address counters.

This capture board was originally designed to handle both physical and logical capture. Physical capture is capturing all voltages from the DUT, governed only by the DUT clock. Logical capture is capturing only what the DUT will write to it. Logical capture, at this time, works and it has been considered unnecessary to use physical capture. Logical capture requires only one memory bank and a data path of only eight bits (as opposed to 24 bits.) If any further development is in logical capture only, the capture memory can be eight bit wide slower (100 nanosecond) memory, and the data path need only be eight bits wide (as opposed to 24 bits.)

Device Under Test

The DUT is subjected to different clock frequencies, illuminated by a controlled laser at various intensities, locations, and times, and made to write data into the capture RAM. Any deviations from an agreed upon test vector will be flagged as a valid failure. This test vector is located in fast ROM to be executed by the DUT. The fast ROM is connected to the DUT to make an environment in which the DUT can operate in. The capture memory receives the bank 1 select and clock from the DUT I/O write signal. The DUT need merely to write to an I/O port and that value will be captured in memory. This is in line with the "logical capture" method described above.

The DUT is mounted in a ZIF (zero insertion force) socket, mounted on the capture and sequencer board, which in turn is mounted on the X-Y stage (Klinger Scientific) under a microscope with objective capable of producing a 2 micron laser spot. For the simple device, the DUT is mounted on a simple socket board on the same stage and under the same microscope as the complex device.

The pair of transistors on the top left of the DUT88 schematic control the power going to the DUT. They disconnect power on command from the controller just in case a valid failure is detected, to protect against possible damage from latchup. They reapply power to the chip before a test sequence.

Sequencer and Clock Circuitry

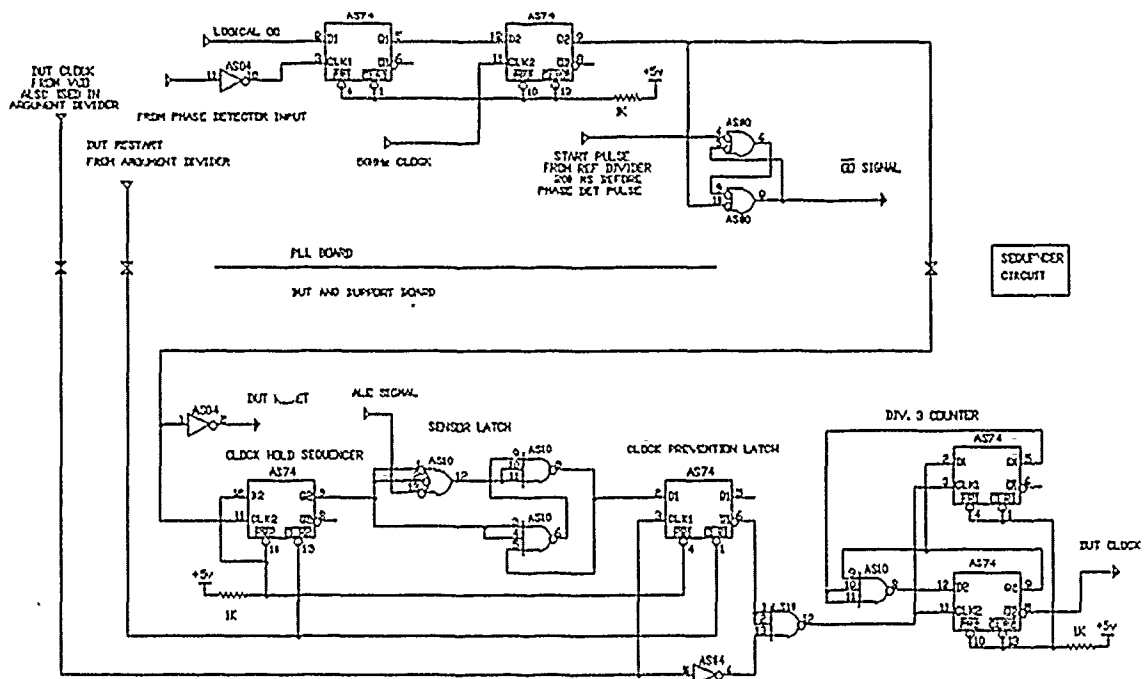
The sequencer operates on all three aspects of the complex device test, except that it is needed only for the state rank test. This circuit is responsible for coordinating the PLL, laser timer, and DUT, so that the laser will consistently illuminate the same logic state on the DUT when the same state delay is programmed into the laser timer.

The PLL has periods, every millisecond (see above under Phase Locked Loop), when the DUT clock and the 50 MHz clock come into convergence. These periods are very phase stable, regardless of DUT frequency, and are relied upon to make consistent the timing between the DUT and its clock with the laser timer, which operates from the 50MHz master clock. Because of this, the laser timer starts only when one of these PLL consistency periods happen. The PLL can then hold the DUT clock and master clock within 2 nanoseconds of each other. This value is small (6 percent) compared to the 33 nanosecond minimum long states of the DUT. Since the signals going to the phase detector are rising edges during this consistency period, it is a simple matter to detect a rising edge at the phase detector and use this as a legitimate GO signal for the laser timer.

The sequence is actually more complex than this, however. The DUT will come out of reset in any state within a logical instruction cycle (the machine instruction cycle of the DUT) and render useless any attempts to coordinate logic states, by use of reset alone. Therefore, some other signal must be used to indicate progress in an instruction cycle, and the laser timer must be coordinated to that signal. The circuit shown on the next page is the sequencer and performs that operation.

The ALE signal from the 8088 is the signal used to coordinate logic states and laser timing. It is a physical signal that tells when a logic state has occurred. The sequencer works like this:

1: A logical GO signal goes to the PLL board from the controller. It has no knowledge of PLL states, and thus must be coordinated to the PLL in some way. The first AS74 latches the GO signal using the phase detector rising edge.



The second AS74 coordinates the logical GO signal with the 50 MHz clock, somewhat cleaning it up. This logical GO signal is not ready for the laser timer, but it is ready to "unreset" the DUT.

2: The DUT "unresets". After a while, an ALE signal arrives, to be picked up by a NAND gate latch and fed into the data input of a third AS74. Upon receiving a rising edge from the DUT clock, the AS74 latches the data from the ALE signal and prevents the DUT from getting clock pulses. The DUT now is in suspension of clock pulses until the PLL has another consistency period.

3: The laser timer starts 200 nanoseconds before the PLL has a consistency period. This is to compensate somewhat for

the delays in the Bragg cell and timer. The 200 nanosecond precognition signal is derived from the 50MHz master clock from the reference divider, and therefore, is entirely consistent with the counters in the laser timer.

4: The PLL outputs another consistency signal. This resets the third AS74 so that the clock can, once again, reach the DUT. It sets the fourth AS74 so that the ALE latch can no longer accept a signal to prevent the clock from getting to the DUT. The DUT operates normally until the test vector is ended, with a laser pulse reaching the DUT some time before.

5: The controller, after some time, ends the GO signal, which resets the first, second, and fourth AS74, and the DUT, thus ending a test. Any noise on the ALE line after reset will be cleared on subsequent PLL consistency cycles.

The clock to the 8088 must be a 33 percent duty cycle signal. This signal is generated by the fifth and sixth AS74's configured as a divide by three counter. This counter is not reset during any sequencer operations, but is denied the clock during the 8088 hold operation between PLL consistency signals.

Appendix VII

SCHEMATICS

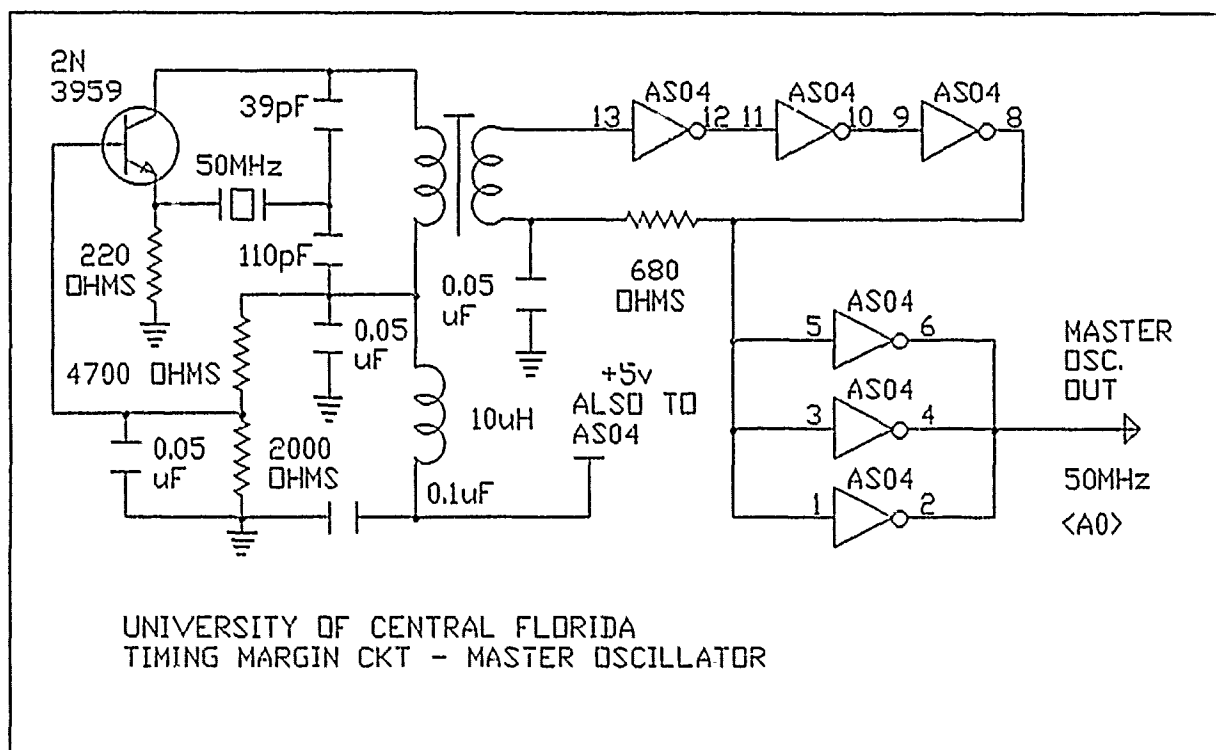
This appendix presents the schematics for both the simple and complex device tests. The controller, master oscillator, both timers, and the propagation delay circuit (receive timer) are used for the simple device test. The PLL, capture, and DUT88 boards are used in lieu of the fixed and receive timers for the complex device test.

The multiple schematics have numbers in packets (<B0> for example) near signal lines. This is an aid for connecting the schematics together. The PLL and receive timer boards should not be connected together, as they use the same address, and therefore, will cause a bus conflict. The GO signal is divided into two parts: <B13A> is the GO signal for the simple device test, and <B13B> is the GO signal for the complex device test. The <B13> signal can connect to either of the signals above, BUT NOT BOTH. Either <B13A>, for the simple device test, or <B13B> for the complex device test is used, BUT NOT BOTH, and <B13> is connected to the needed signal. Both cannot be used, as a bus conflict will occur.

The lettering for these signal labels follows closely with the function of the circuitry concerned. For example, B for Bus, R for Receive timer, T for Timing line, C for Capture line, and so forth. A stands for master oscillator.

The variable timer output ALWAYS goes to the Bragg cell modulator. D6 at address A07 on the variable timer (not mentioned on register set map) is used to switch an inline filter into the signal path to the modulator. A schematic will not be presented of the filter, but suffice it to say that the filter rejects anything above 50kHz, differential and common mode, when activated. This filter is used to cleanse the signal going to the Bragg cell modulator, when in complex device node rank mode.

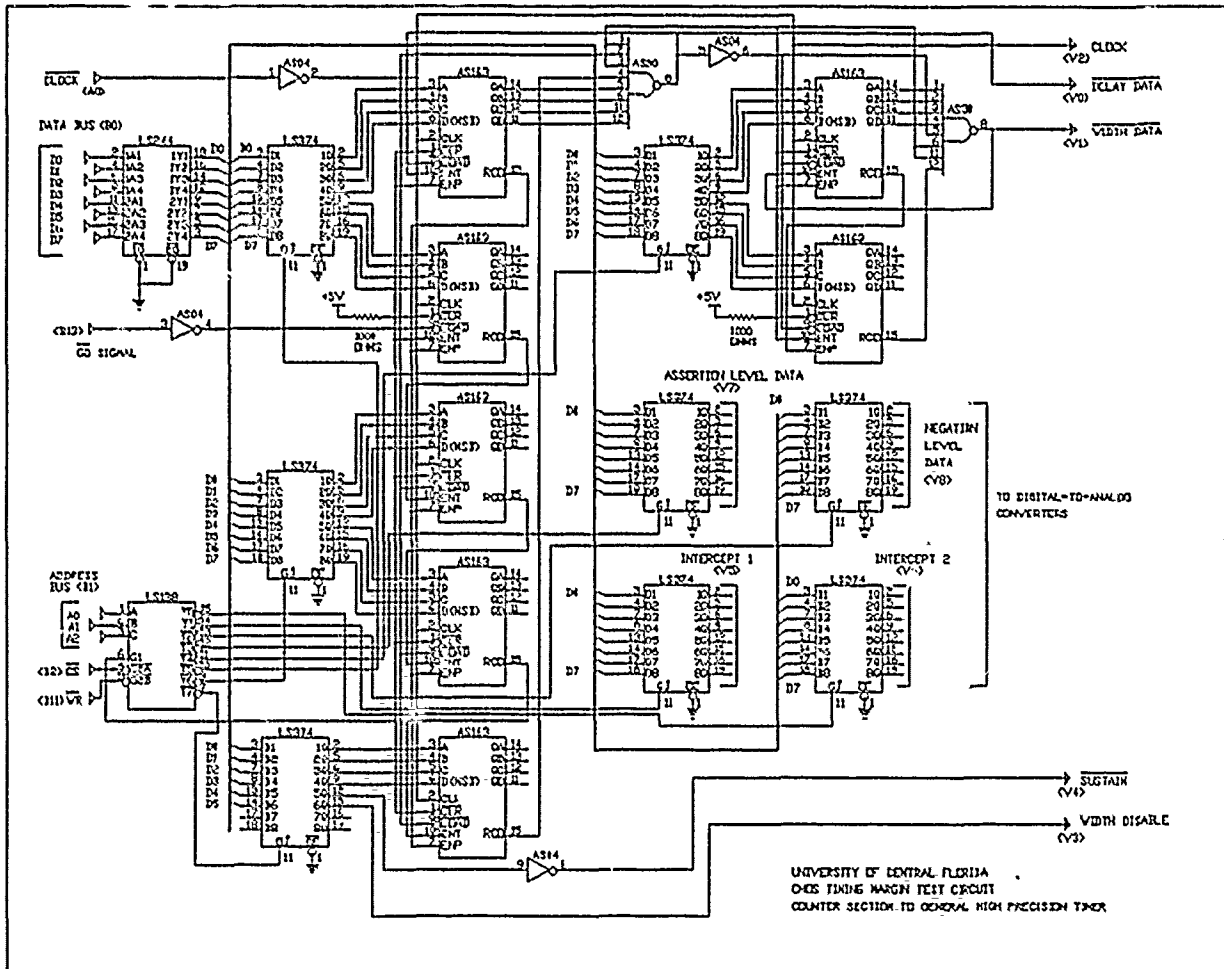
Connecting the complex device into the test circuitry is self explanatory (DUT88.DXF), but no schematic mention is made for connecting the simple device. The input of the inverter or gate is connected to two points: The first, which is a 50 ohm coax, is the output of the fixed timer. The second point is one of the inputs of the receive timer (propagation delay), and is connected through 1000 ohm impedance "spider" wire as close as possible to the DUT. The output of the inverter or gate is connected through the same type and length of "spider" wire to the other input of the propagation delay circuit. For this test, the "spider" wire was 6 inches long.



(osc.dxf)

This schematic is to the Master 50MHz clock oscillator needed to properly time all of test electronics. Both the fixed and variable timers need this clock for the simple device test. For the complex device, the variable timer and PLL need this clock for a reference.

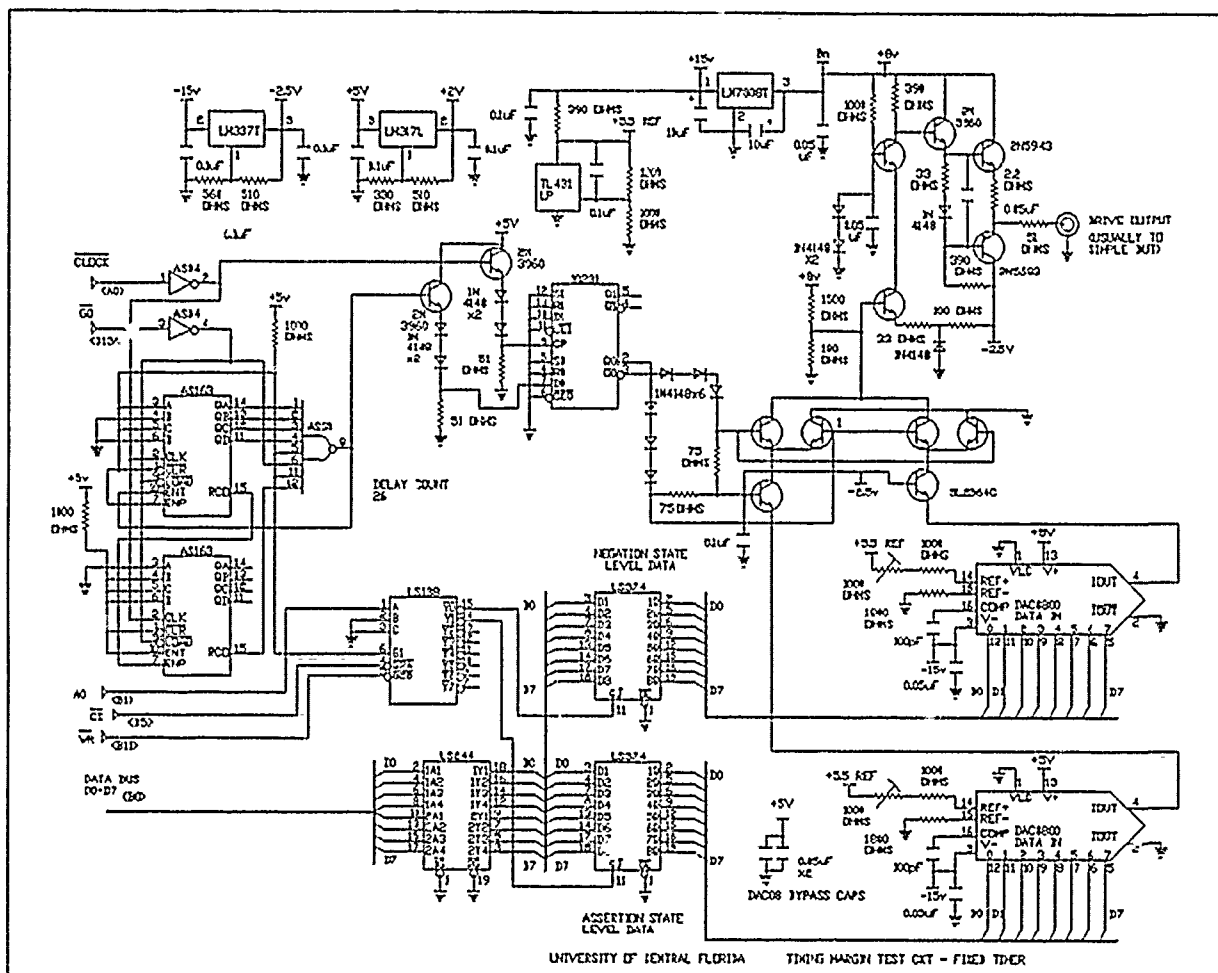
Test Bed Usage: Simple and Complex Devices.



(vtmr2.dxf)

This schematic deals with the digital part of the variable timer.

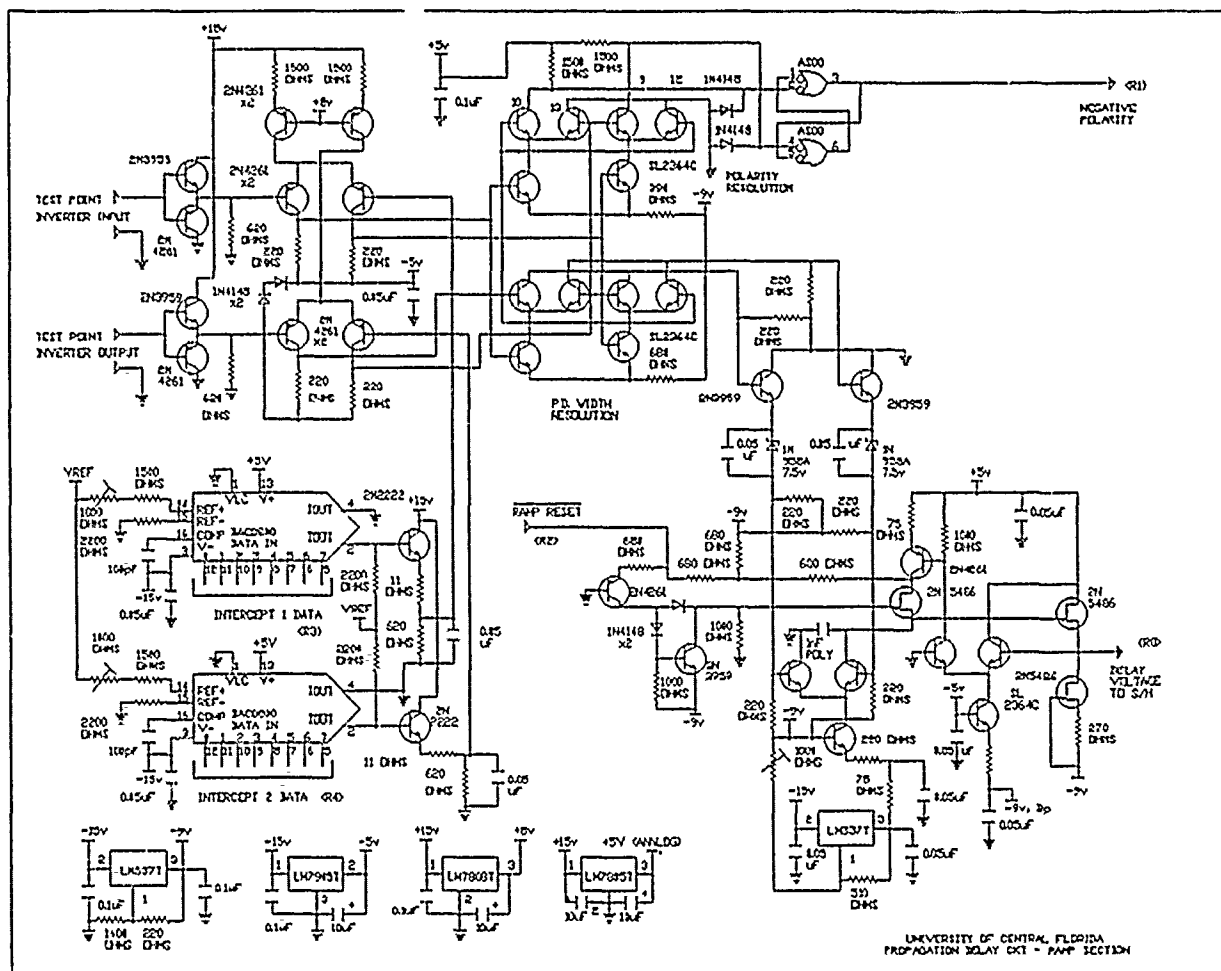
Test Bed Usage: Simple and Complex Devices.



(ftimer.dxf)

This is the fixed timer that gives a signal to the input of the simple device under test. It delays the GO signal by a fixed amount (knowledge of its value unnecessary), and then causes to switch current and built-up voltage in the same manner as the ramp section of the variable timer.

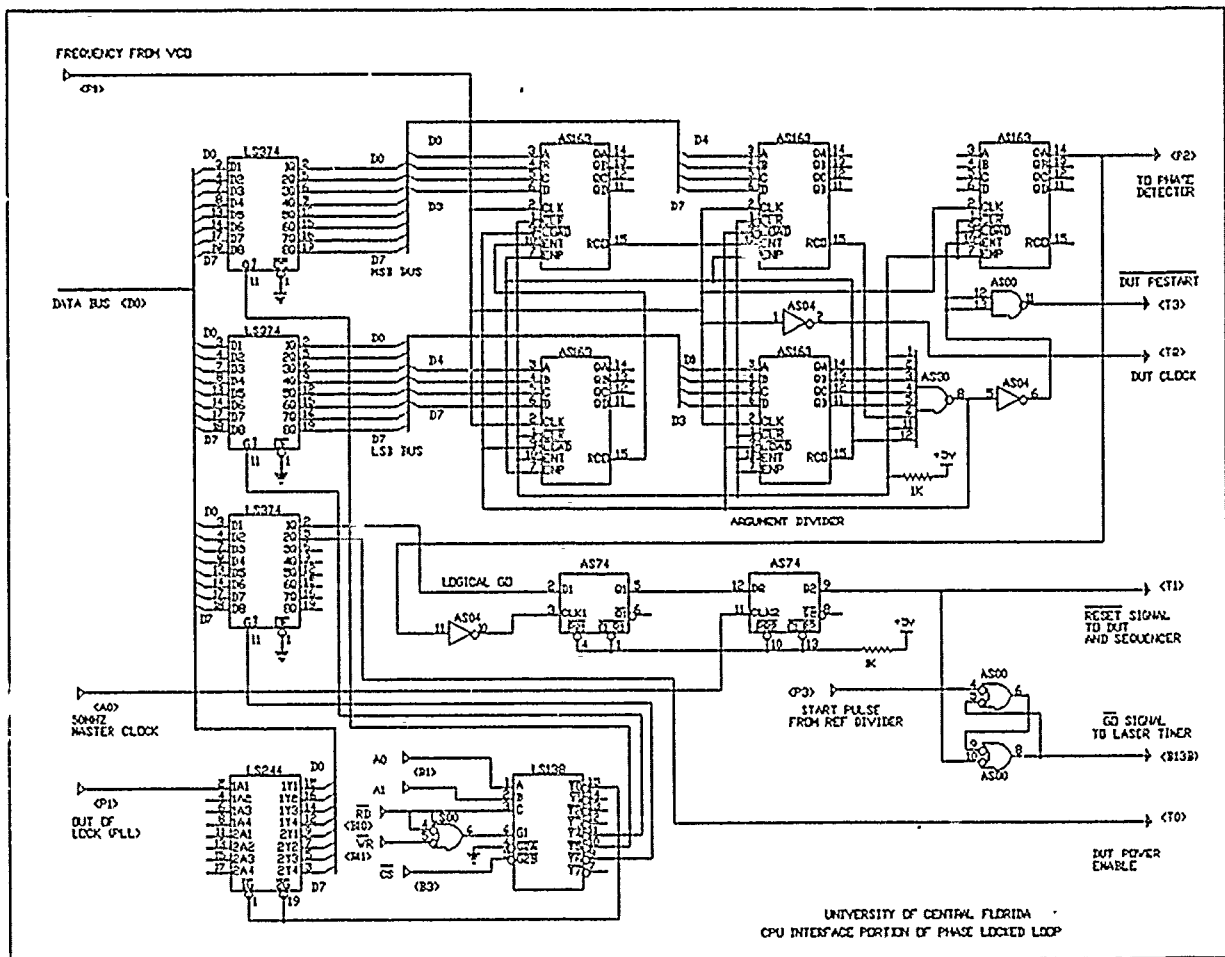
Test Bed Usage: Simple Device Only.



(rtmr1.dxf)

This schematic deals with the circuit that measures the propagation delay of a simple device. This circuit gates a current for the duration of the propagation delay and ramps a voltage from this current. The voltage out of this ramp is proportional to the propagation delay.

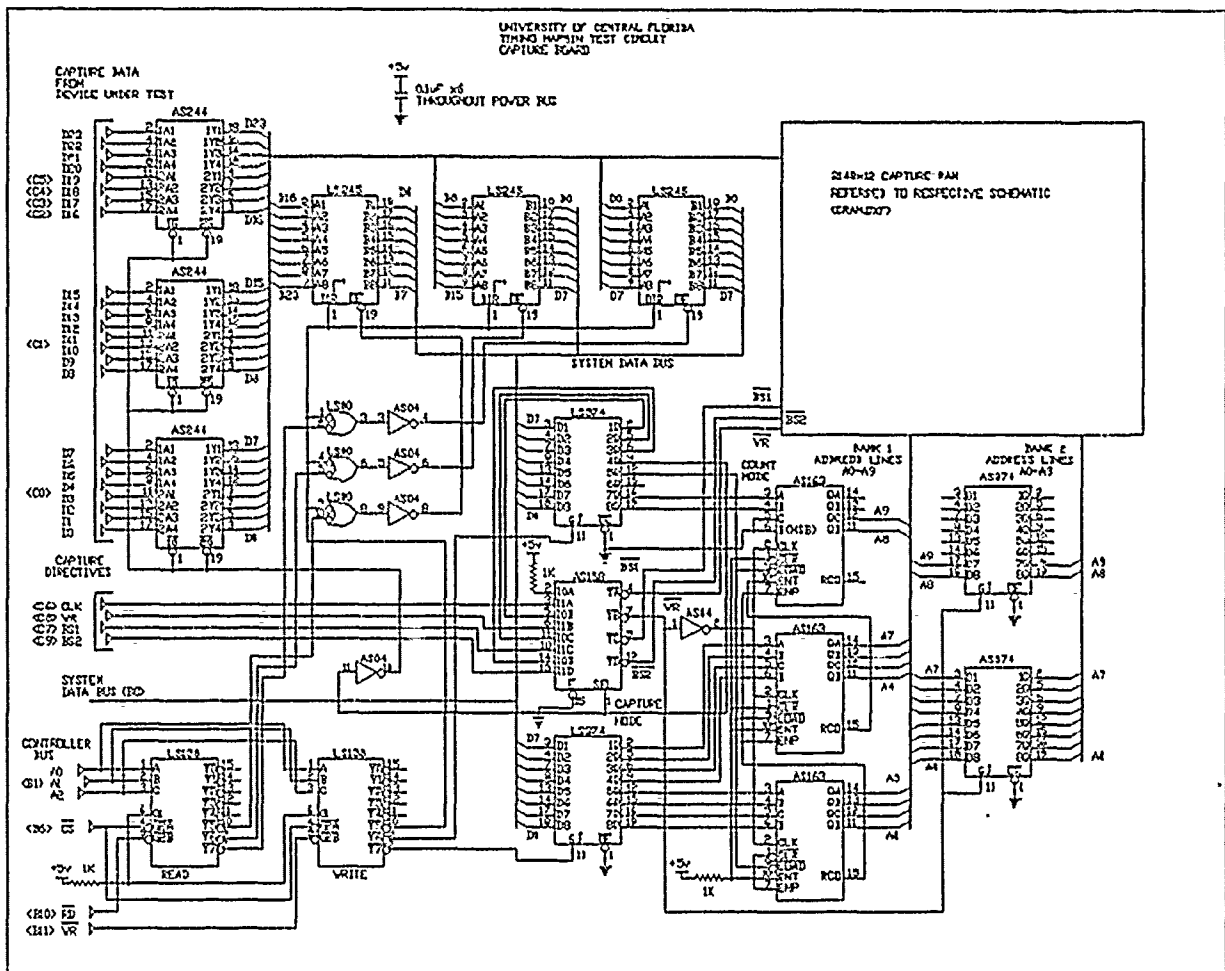
Test Bed Usage: Simple Device Only.



(pll2.dxf)

The circuit in this schematic handles part of the frequency synthesis operation for the complex device test, and some of the complex device sequencing.

Test Bed Usage: Complex Device Only.

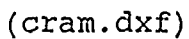


(capture.dxf)

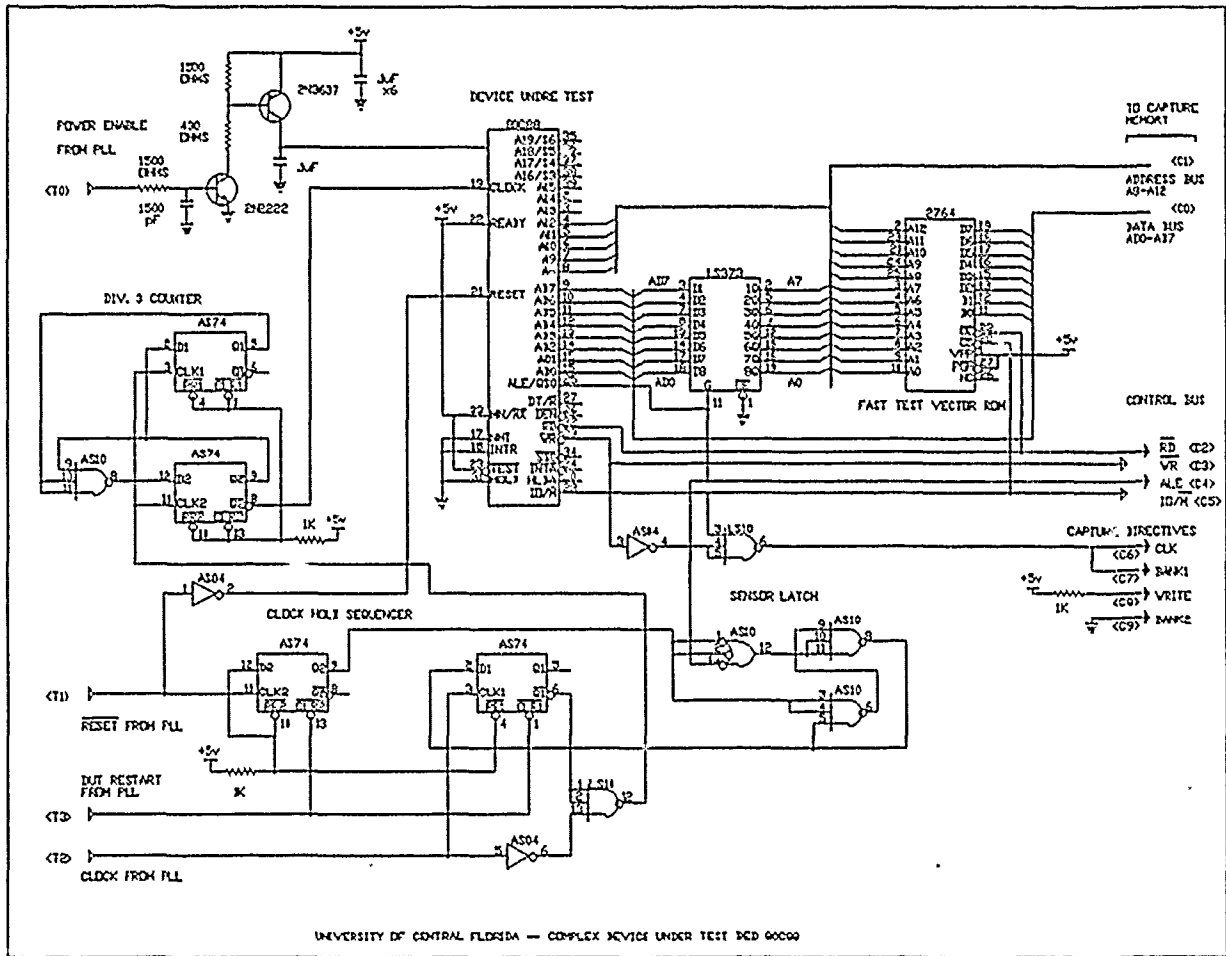
This circuit captures the test states from the device under test. Provision have been made to reset the memory (shown as a block) before a capture. The logical capture that this memory receives can come from a device under test that can operate up to 22 MHz.

Test Bed Usage: Complex Device Only.

15V
0.35 MΩ
DISTRIBUTED THROUGH-OUT CIRCUIT



Test Bed Usage: Complex Device Only.



(dut88.dxf)

This is the DUT and immediate (required) test bed electronics. The ROM chip to the right (2764) has the test vectors. The circuitry under the DUT in cooperation with the PLL circuitry handle hardware sequencing requirements to properly align the DUT state timing with the laser timing.

Test Bed Usage: Complex Device Only.



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